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DESIGN AND DEVELOPMENT OF CASCADED MULTILEVEL INVERTER USING GENETIC ALGORITHM

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Abstract— *Super-capacitors and MLIs are commonly used energy storage devices in electrical vehicle applications.While rechargeable batteries have high capacity and low leakage rate, the relatively short cycle life limits the lifetime of sensor nodes. On the other hand, Super-capacitors have certain advantages such as longer cycle life and higher charge-discharge efficiency. Super-capacitors can be characterized using electrochemical impedance spectroscopy, which is a widely used approach to characterize energy buffers. Researches done based on basic inverter topologies show that multilevel inverters (MLIs) have many advantages, such as low power dissipation on power switches, low dv/dt ratios, low harmonic and low electromagnetic interference (EMI) outputs.*

Keywords— Super-capacitors, MLI, low dv/dt ratios, low harmonic ,low electromagnetic interference

I. INTRODUCTION

Popular MLI topologies have already been examined to define most appropriate structure for Sinusoidal Pulse Width Modulation (SPWM) strategy. The best answer is cascaded H-bridge according to observations. As the next generation of automotives are becoming more and more complex in terms of operation, calculation for those operation is a major task. So it is important to use the inverter system which is more efficient. There is a need to design a inverter system using super-capacitors or multiple level inverters for use in E-vehicles using renewable energy sources like Solar equipment. Currently, there is requirement for state- of- the- art conversion from DC to AC for use in increased power and power quality needed applications. There is a compelling need for a Multilevel converter which can reduce the total harmonic distortion increasing the system efficiency. Also, a reduction in the cost and size of the converter improving power quality is necessary. Hence there is a need to design a power system using Super-capacitors or multiple level inverters for use in E-vehicles using renewable energy sources like Solar/wind energy. In this project, different circuits have been constructed for which the output has been analyzed.

Objective is to design a multilevel inverter which depends on renewable energy preferably using Super-capacitors, to increase the power quality and dynamic stability for utility systems, to obtain very high efficiency (>98%) by use of minimum switching frequency. Cascaded H-bridge MLI (CHBMLI) topology consists of series of power conversion cells and power to be easily scaled. Cascaded H-bridge MLI (CHBMLI) is simulated with novel PWM techniques to reduce the number of passive elements, Total Harmonic distortion (THD) and to increase efficiency. A Novel PWM technique is implemented in MATLAB-SIMULINK to analyze the performance of multilevel inverter. Finally, the Software Implementation of cascaded H-Bridge multilevel inverter is according to genetic algorithm. In this project, different circuits have been constructed for which the output has been analyzed. In this work, genetic algorithm has been included for in depth study of the output. In summary, work for this project include Super-capacitors in EV circuit, attach the HBridge circuit and use genetic algorithm to analyze the output. Learning outcomes of the project include learning the EV architecture, hands on experience with the Simulink tool, creation of circuits, generating and analyzing outputs.

Use of new technology to reduce energy consumption and reduction has become an important direction in the development of the automobile industry, and electric vehicle has become an attractive solution for energy saving and reduction in emission [1].

Methodology

Methodology is as follows:

1. Cascaded H-bridge MLI (CHBMLI) topology consisting series of power conversion cells and power to be easily scaled[5].

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2. Cascaded H-bridge MLI (CHBMLI) can be simulated with novel PWM techniques to reduce the number of passive elements, Total Harmonic distortion (THD) and for increasing efficiency.

3. A Novel PWM technique is implemented in MATLAB-SIMULINK to analyze the performance of multilevel inverter .

4. Software Implementation of cascaded H-Bridge multilevel inverter according to genetic algorithm.

. Constraints

This project work carried out takes careful account of all key constraints which includes lack of option in the Simulink for response optimizer exists but absence of genetic algorithm.

I. CHALLENGES

A. Research Gap

1. Switching currents and switching angles both are analyzed here compared to previous research where only switching angles are concentrated on. Here, equal weightage is given to both.

2. In previous papers, Newton Raphson Method is used to solve the above non linear transcendental equations (1) to (4) and find the switching angle [3].

3. Newton Raphson Method is time consuming and equations need to be solved whereas genetic algorithm can easily be implemented .

4.Here, genetic algorithm selects the individuals at random rather than involving more mathematical calculations.

B. Problem Analysis

1) Genetic algorithm is used for analysis of the problem.

2) Newton Raphson Method can be used to solve the nonlinear transcendental equations(1) to (4) . This should autogenerate the switching angle.

3) Due to mathematical calculations in this method shown above complicating the process, it consumes some time.

4) GA selects the individual randomly. Each individual is paired with another individual and assigned as parent. Next, can calculate value of the child for successive generation.

5)Thus, population will gradually evolve and move to optimal solution comprising generations one after the other.

6) In GA, switching angles are selected random and generation as well as population indices are to be computed. Along with this, for the individuals an objective function has to fall within threshold so that only the best can be selected.

7)Once converging happens, Switching angles are got so that it does not repeat to get another successive generation. 8)Variables to be entered are 4 here. Start button to be clicked after finding fitness (total harmonic distortion). When iterated value, population index, generation index are to be varied and optimum values of switching angle is found. Iteration counts also will be variedUnits

B. Equations

v1rms=[4/sqrt(2*pi)](VB1*Cos(ϴ1)+VB2*Cos(ϴ2)+VB3*Cos(ϴ3)+VB4*Cos(ϴ4)) ----------------------------------(1)

v3rms=[4/sqrt(23*pi)](VB1*Cos(3ϴ1)+VB2*Cos(3ϴ2)+VB3*Cos(3ϴ3)+VB4*Cos(3ϴ4)-----------------------------(2)

v5rms=[4/sqrt(25*pi)](VB1*Cos(5ϴ1)+VB2*Cos(5ϴ2)+VB3*Cos(5ϴ3)+VB4*Cos(5ϴ4)-----------------------------(3)

v7rms=[4/sqrt(27*pi)](VB1*Cos(7ϴ1)+VB2*Cos(7ϴ2)+VB3*Cos(7ϴ3)+VB4*Cos(7ϴ4)) ---------------------------(4)

where 0<ϴ1<ϴ2<ϴ3<ϴ4<pi/2

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C. **Test Design and Hardware**

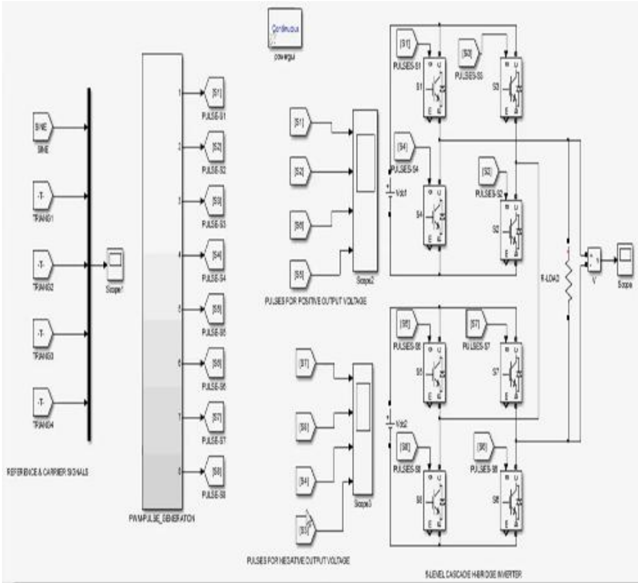

Fig 1.1: 5-level cascade HBridge inverter

Fig 1.1 shows the block diagram of a 5-level cascade H-Bridge inverter.

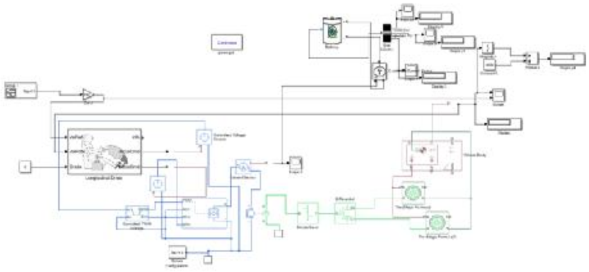

Fig 1.2: Electric Vehicle Circuit

The Electric Vehicle Circuit is as shown in fig 1.2 consists of components like scope, controlled PWM voltage, battery etc

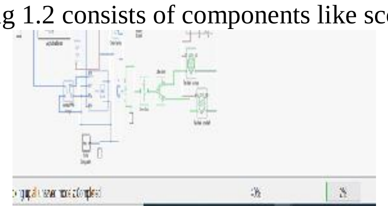

Fig 1.3: Testing The Circuit

As shown in fig 1.3 the circuit has been tested successfully and obtained value of 58 km/hr.

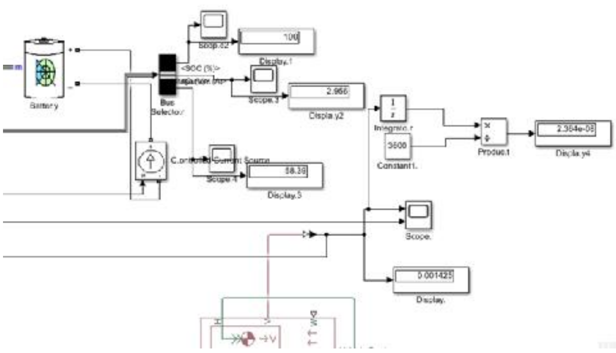

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Fig 1.4: Output Values On Display And Scope Units

The output obtained from the EV circuit is as shown in the fig 1.4 . After successful compilation, we can obtain speed of 58 km/hr.

II. DESIGN

- Excellent design and meets all functional requirements;
- Flexible design can accommodate potential future changes like a genetic algorithm which has potential to calculate for higher levels of the inverters requiring a different design in only the hardware.
- Takes careful account of all key constraints which includes lack of option in the Simulink for response optimizer exists but absence of genetic algorithm.

A. Implementation

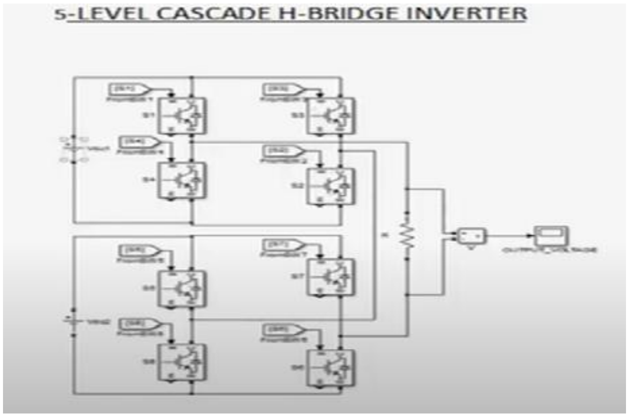

Fig 1.5: 5 level cascade H Bridge Inverter

As shown in Fig 1.5, 5 level cascade H Bridge Inverter can be constructed by following steps:
1.Grab all components into our new model
2.Design the circuit shown. It is the main circuit of 5level cascaded Hbridge inverter
3. Start with IGBT switch as 1st component
4. Drag and place all the components in similar manner.

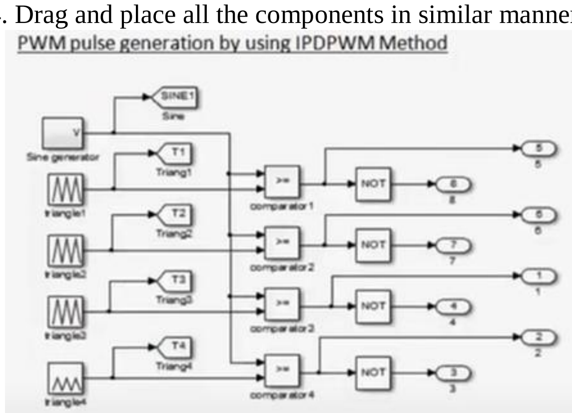

Fig 1.6: PWM pulse generation by using IPDPWM Method

As shown in Fig 1.6, In SPWM method, a reference signal compared with high frequency carrier signal to generate PWM pulses to the IGBT Switches of multilevel inverter[4].
Reference signal taken as sinusoidal waveform(x1) and carrier as triangular waveform(x4).2 carrier are below 0 and 2 are above 0.
No of carrier signals required =m-1

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M=no.of level
For 5 level, no of carrier signals=4
Reference signal=1
Here IPDPWM used, all carrier above and below zero reference line are in same phase .
All reference and carriers are arranged like this below:

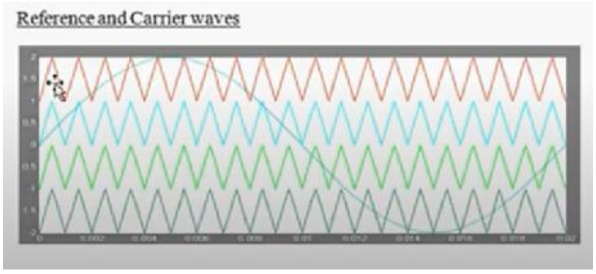

Fig 1.7: Reference And Carrier Waves

As shown in Fig 1.7,all Carrier signals are in phase
By changing/controlling apmplitude and freq of carrier and reference , can control harmonic in the output.

The frequency modulation index mf = fc/fm
The Amplitude modulation index ma = Am/ (m-1) Ac
Where fc – Frequency of the carrier signal
fm – Frequency of the reference signal
Am –Amplitude of the reference signal
Ac – Amplitude of the carrier signal
m – Number of levels.

Fig 1.8: Frequency Modulation Index And Amplitude Modulation Index

As shown in Fig 1.8,Take fc=10khz Am=2
Fm=50hz, Ac=2
Mf=10000/50=200,Ma=2/[(5-1)2]=0.25
For 50hz freq, time per cycle=1/50=0.02 s
For 10khz freq=1/10000=0.0001s

Pulse no.	Vdc	2Vdc			Vdc	-Vdc	-2Vdc			-Vdc
Angle	30^0	60^0	120^0	150^0	180	210	240^0	300^0	330^0	360
Time(Sec.)	0.00166	0.0033	0.0066	0.0083	0.01	0.01166	0.0133	0.0166	0.0183	0.02
S1,S2&S6	ON-PERIOD PULSE WIDTH									
S5		ON-PERIOD PULSE WIDTH								
S7,S8 & S4						ON-PERIOD PULSE WIDTH				
S3							ON-PERIOD PULSE WIDTH			

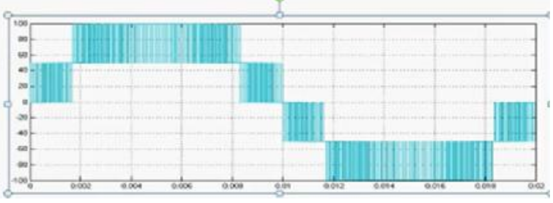

Fig 1.9: Output Of 5 Level Inverter

As shown in Fig 4.4,+Vdc Portion Is From 0 To 40V By Turning On S1,S2,S6.

2vdc Portion Got By Turning On S1,S2,S5,S6.

Again ++Vdc Portion Got By Turning On S1,S2,S6.

-Vdc Portion From 0 To -50v By Turning On S7,S8,S4.

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-2vdc Portion By Turning On S7,S8,S4,S3.

-Vdc Portion By Turning On S7,S8,S4 For 0 To -50V.

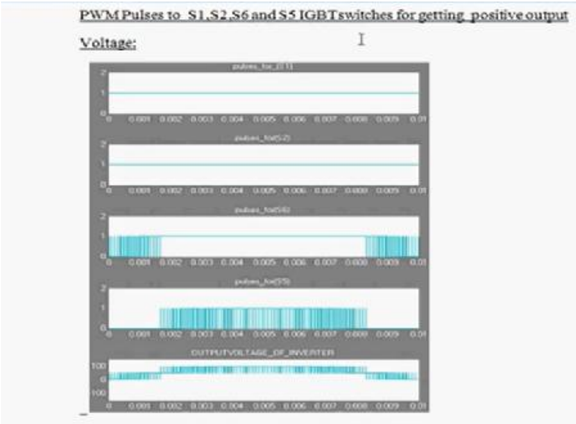

Fig 1.10: Positive Output Voltage

As shown in Fig 1.10, For getting positive output, have pulse for S1,S2,S6,S5 Respectively.end result positive output of inverter, Ie, Vdc Portion, 2Vdc Portion And Vdc Portion . Pulses to S1,S2 CONTINUOSLY ON, but on condition of switch for S6,S5, output of inverter is decided.Both keep going on and off.Vdc Follows S6.Output Portion Pulse Width Of S6 Are Same.To Get 2vdc Output Portion , Turn On S1,2,5,6 , Pulse To S5 Not Continuous, Based on On N Off Condition Of S5, 2vdc Portion Of Output Voltage

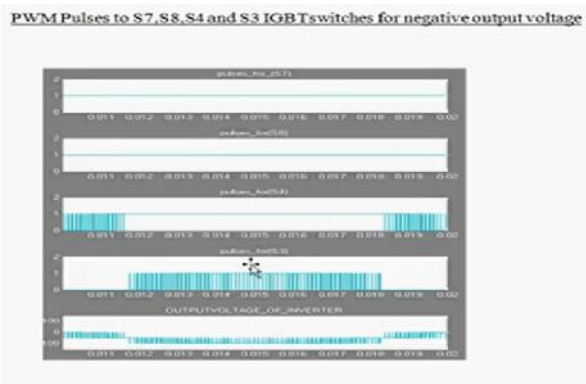

Fig 1.11: Negative Output Voltage

Fig 1.11 shows Pulses to S1,S2 CONTINUOSLY ON, but on condition of switch for S6,S5, output of inverter is decided.Both keep going on and off.Vdc Follows S6.

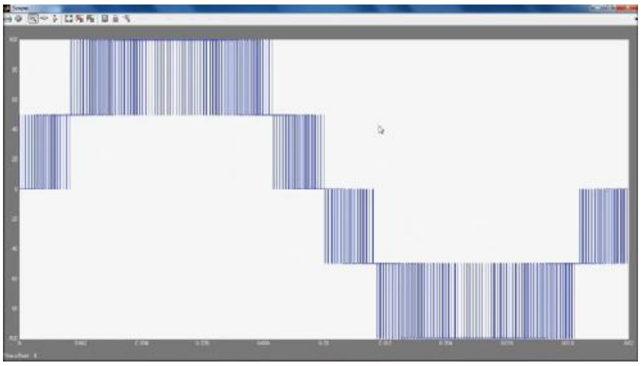

Fig 1.12: Desired output

Fig 1.12 shows output portion pulse width Of S6 Are Same.To Get 2vdc Output Portion , Turn On S1,2,5,6 , Pulse To S5 Not Continuous, Based on On N Off Condition Of S5, 2vdc Portion Of Output Voltage

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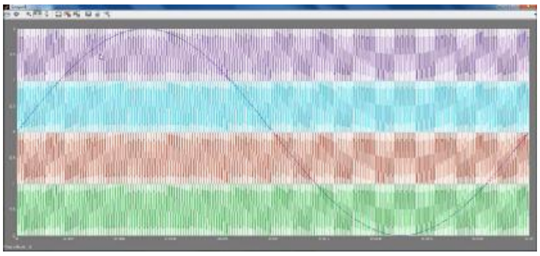

Fig 1.13: Input Reference And Carrier Waves

Fig 1.13 shows Reference signal taken as sinusoidal waveform(x1) and carrier as triangular waveform(x4).2 carrier are below 0 and 2 are above 0.

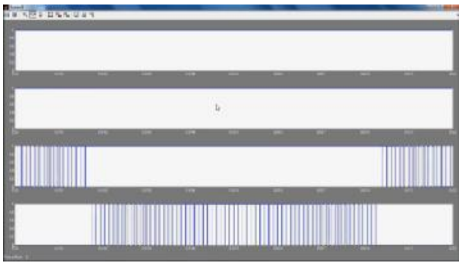

Fig 1.14: Vdc and 2Vdc wrt carrier signals

Fig 1.14 shows the signals already explained in proper format ie, Vdc and 2Vdc wrt carrier signals.

B. Results

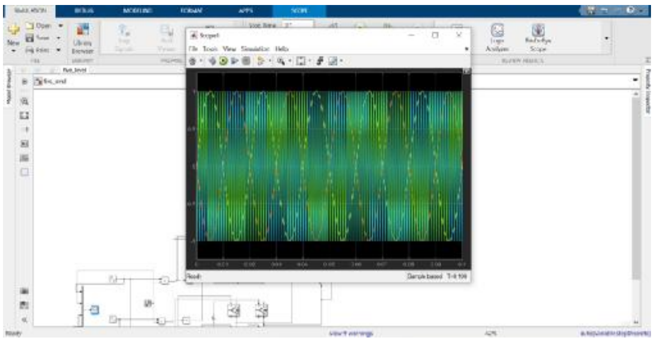

Fig 1.15: Reference And Carrier signals Input to cascaded inverter measured on Scope display

Fig 1.15 shows Reference And Carrier signals Input to cascaded inverter measured on Scope display

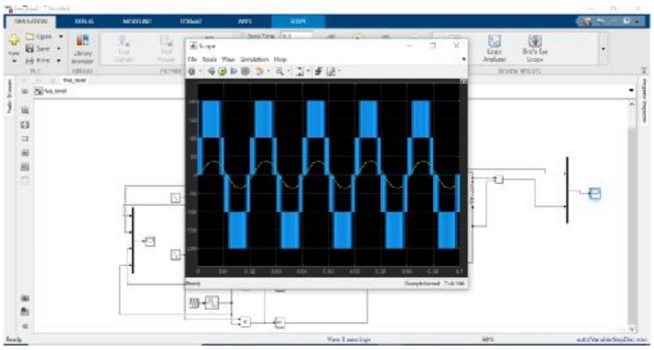

Fig 1.16: Obtained output from inverter circuit

As shown in Fig 4.14 above is obtained output from 5 level cascaded inverter circuit, output is taken from the blue color scope as marked in figure 1.16.

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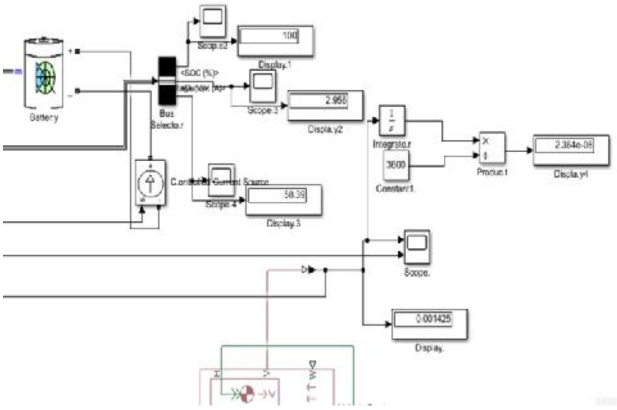

Fig 1.17: Obtained output from EV circuit

As shown in Fig 1.17 battery is used for EV circuit, which will be replaced by super-capacitor in phase 2. The outputs are taken from the display unit attached to the scope. To calculate average speed manually, divide distance by time, our speed is approx. 50km/hr. actual speed is trying to follow the reference speed. Meticulous implementation of this design is following a standard process with optimal resource usage.

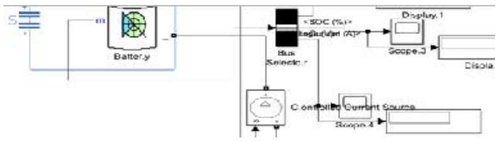

Fig 1.18: Addition of supercapacitor

As shown in Fig 1.18, addition of supercapacitor is made to the circuit.

```
effectsga.m  fitnessGA.m  mainGA.m  +
rng default % For reproducibility
fun = @(x)log(rastriginsfcn(x));
nvar = 10;
```

Fig 1.19 Use Of Genetic Algorithm Code For Implementation

As shown in fig 1.19, use Of Genetic Algorithm code for implementation is necessary.

Optimum angles are found by The program which minimizes till the 6n+1th harmonics using genetic algorithm.

The following are the functions

1."fitness.m" for population fitness calculations

2."mainmenu.m" displays menu to select option from large list

Levels 2n+1 exists for cascade of upto n converters. Answer is acceptable if the percent of harmonic sum of selected in particular –those harmonics have sum less than minute . The number of iterations as well as points will be not matching for those solutions which are unacceptable.

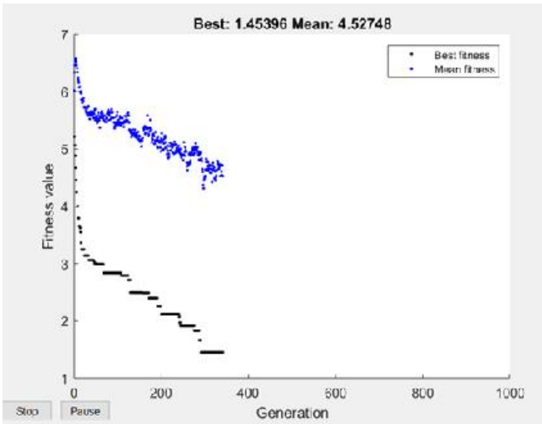

Fig 1.20 Obtained output displaying fitness value according to generation

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As shown in fig 1.20, genetic Algorithm with initial values in random is suggested for solving the transcendental nonlinear equations known as Selective Harmonic Elimination equations that characterize the selected harmonics . Low modulation indices [0, 0.256], high modulation indices [0.934, 1] .No solution sets are existing for few modulation indices. There will be absence of a solution set for those modulation indices or could not be found.
The THD in line-to-line voltage as computed analytically and from simulation .The analytical and simulation values of THD are in close agreement thereby validating the analytical results[5].

The proposed method is derivative-free, accurate and globally convergent. Selected harmonics are not present in the synthesized output phase voltage. This is used to validate results.

```
% Evaluates the fitness of the chromosomes
function [sol, val] = fitnessGA(sol,~)
global harm_n
M=sol;
N=4096; %N is a power of 2
kk=max(size(sol))-1;
V=125*ones(1,kk);
[fftvao , ~]=modulation(N,M,V);
vv=abs(fftvao(2));
sumh=0;
for g=1:harm_n
 h5=abs((fftvao(6*g+1+1))); %(6n+1)th harmonic
 h7=abs((fftvao(6*g-1+1))); %(6n-1)th harmonic
 sumh=sumh+h5+h7;
end
val=-100*(sumh)/vv;
```

Fig 1.21 Function Used To Evaluate Fitness

As shown in Fig 1.21 function used to evaluate fitness and suitable values of N taken such that it is power of 2.

```
Command Window
>> effectsga
Optimization terminated: average change in the fitness value less than options.FunctionTolerance.

x =

  Columns 1 through 5

   -0.0495   -0.0670   -0.0405    0.0174   -0.0087

  Columns 6 through 10

    0.0275   -0.0353    0.0620   -1.0047   -0.0258


fval =

    1.4540

>>
```

Fig 1.22 Command window displays fval value.

As shown in Fig 1.22 ,the option determines the maximum number of generations the genetic algorithm takes, successfully validating the results.

E. Future Scope

Future work for this project is hardware implementation of the electric vehicle using the same features and testing in a suitable environment.

CONCLUSION

In this project, different circuits have been constructed for which the output has been analysed during Phase 1 of the project. In this project, different circuits have been constructed for which the output has been analysed. In future work,ie,Phase 2, genetic algorithm will be included for in depth study of the output. Speed of 58km/hr is obtained in the EV circuit which is close to the desired average speed of the Evehicle which is about 50 km/hr as per the average. Through the use of a multilevel inverter specifically designed using genetic algorithm, multilevel inverter outputs can be analysed for desired combinational sequence of the output current values which can lead to a better design. Also, supercapacitor usage in the circuit of the electric vehicle can bring about major changes to the circuit when introduced with a multilevel circuit which analysed using genetic algorithm in Simulink,can act as further improvement to the existing project.. For phase 1, EV circuit was designed with a view to attach a new form of inverter in the next phase 2 stage of project and now, incorporated the same in the EV circuit and finally tested it using Genetic Algorithm.

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