Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )

Volume 5- Issue 1, Paper 36 January 2022

# DESIGN OF D FLIP – FLOP USING KISAN GATE

Kirankumar Manivannan Dr.M. Santhi,Jennithra.S Iniya.R
Student, Department of ECE,
Easwari Engineering College,
Chennai, iniyaramesh132@gmail.com

## ABSTRACT

D Flip-flops are sent anyplace in a remote sensor organization. So their correspondence can be effortlessly checked. In these organizations, message security and hub recognizable proof are normal issues. Consequently, security of enormous scope such organizations requires proficient key dissemination and the board systems. Significant steganography and especiallysignificant key dispersion is such a procedure that dispenses secure keys just for brief distances. The significant steganography offers enormous benefits over conventional strategies by the utilization of trash yield decrease and significant transmission, even thoughit is not totally secure. These issues can be recuperated by utilizing the reversible rationale entryways in effective way. Here another reversible 4x4 rationale entryway called KISAN door has been utilized. This has been joined with QKDP to accomplish secure correspondence in WSN. In our examination, we embraced C-R plot as far as these significant entryways to defeat the weakness brought about by noxious hubs. As the qubits put away in a sensor hub can be utilized just a single time and can't be copied, subsequently hazard of data spillage diminished regardless of whether the hub are compromised.

***Keywords –*** D Flip-flops, KISAN gate, QKDP, Cryptography

## I. INTRODUCTION

Reserve power, additionally calledvampire power [1], vampire draw,apparition load, ghost load or spilling power ("apparition load" and "spilling power" are characterized specialized terms with different implications, embraced for this different reason), alludes to the manner in which electric power is consumed by electronic and electrical machines while they are turned off (yet are intended to drawsome power) or in backup mode. This just happens on the grounds that a few gadgets professed to be "turned off" on the electronic point of interaction, however are in an alternate state from turning off at the attachment, or separating from the power point, which can tackle the issue of backup power totally. Indeed, turning off at the power point is sufficiently compelling, there is no compelling reason to disengage all gadgets from the power point. Whatever gadgets offer controllers and advanced clock elements to the client, while different gadgets, like power connectors for detachedelectronic gadgets, consume power without offering any elements (in some cases called

no-heap power). All of the above models, for example, the controller, computerized clock capacities and-on account of connectors, no-heap power-are turned offby turning off at the power point. In any case, for certain gadgets with worked in inside battery, for example, a telephone, the backup capacities can be halted byeliminating the battery all things considered.

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )

**Volume 5- Issue 1, Paper 36 January 2022**

In present day innovation, in advanced plan, energy misfortune is a significant thought. Conventional rationale circuits are tracked down irreversible rationale and disperse heat energy in a request KTln2 joules that the deficiency of per piece of data, where k(K=1.3806505*10-23JK- and T )is outright temperature. Bennett shows that if there should be an occurrence of reversible rationale calculation KTln2 joules energy won't disseminate. Henceforth reversible rationale configuration normally gets need to plan combinational also consecutive circuit. Information are not misfortune in reversible circuits. Reversible doors are needed to plan reversible circuits. Inversion doors are the structure blocks for reversible circuits, having the accompanying attributes.

- A reversible entryway has equivalent information and result to have balanced planning. So the contributions of a reversible door can not set in stone from its results.
- In a reversible entryway fan out of each sign including essential sources of info should be one.
- Traditional strategies for union of a rationale can't be straightforwardly applied to plan reversible rationale circuit.

Trash yield is one of the main elements of a reversible entryway. Each entryway yield that isn't utilized as contribution to other door or as an essential result is called trash yield. Every reversible door is related with an expense called significant cost. The significant cost of an adjustable door is the quantity of 2x2 revocable entryways or significant rationale doors obligatory in planning it.

Reversible rationale is a kind of rationale which has been gotten in various circuits in light of its significant responsibility in the power savingphilosophy [1]. Power spread element and information adversity has been particularly displayed before by the expert Landaurer, who uncovered that the circuit which incorporates any computational part will scatter the energy in the extent of KTln2, where,

'K' → Boltzmann steady, 'T' → temperature and

$ln_2$ → incorporates the proportionality reliable.

Unequivocally the KTln2 variable would have been overlooked whatever amount as could sensibly be anticipated and this kind of recklessness couldn't be refined by standard reasoning styles. While the reversible reasoning has been accepting an enormous part in arranging dispersal free circuits, thusly our all-out spotlight would be on the reasoning style and the ways to diagram the information setback free circuits. Entrances are basically used as building Solid State squares of by far most of the combinational and progressive circuits.

The major flip lemon from other timed types is the D flip failure. It ensures that two sources of information, S and R, are never equal to one at the same time. Fig:1 illustrates the block diagram of D-Flip flop. The Delay flip-flop is designed using a gated SR flip-flop and an inverter connected between the data sources, with a single data D. (Data). This single information input, which is named as "D" utilized instead of the "Set" input and for the corresponding "Reset" input, the inverter is utilized. In this manner, the level-delicate D-

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )
Volume 5- Issue 1, Paper 36 January 2022

type or D flip lemon is developed from a level-touchy SR flip failure. So here S=D and R= ~D(complement of D)

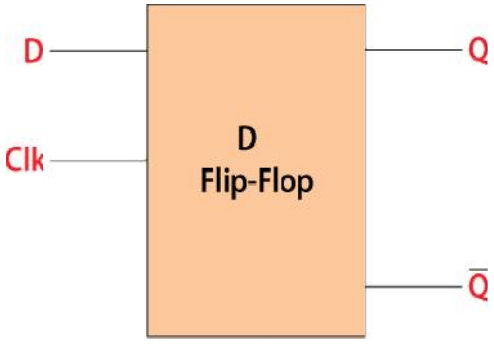



***Fig:1 Design of D Flip - Flop***

## II. Related works

Sensor hubs are sent anyplace in a remote sensor organization. So, their correspondence can be effectively observed. In these organizations, message assurance and hub ID are normal issues. Subsequently, security of enormous scope such organizations requires effective key dissemination and the board components.

Significant cryptography, particularly significant key propagation, is a system that assigns safe keys for only short lengths. While it isn't completely safe, it has a lot of advantages over traditional waste management systems, such as reduced garbage production and substantial transmission. These issues can be recuperated by utilizing the reversible rationale entryways in proficient way. Here another reversible 4x4 rationale door called BKG entryway has been utilized. This has been consolidated with QKDP to accomplish secure correspondence in WSN. In our examination, we embraced C-R conspire as far as these significant doors to conquer the helplessness brought about by noxious hubs. As the qubits put away in a sensor hub can be utilized just a single time and can't be copied, consequently hazard of data spillage diminished regardless of whether the hub are compromised

In late year's reversible rationale has been considered as a significant issue for planning low power advanced circuits. This has driven many investigates to view reversible rationale extremely in a serious way in building significant circuits connected with low power CMOS plan, optical data handling, DNA figuring. The primary reasons for planning reversible rationale are to diminish the quantity of doors, trash results, and power utilization.

Since the result of a consecutive circuit relies upon the current contributions as well as on the past information conditions, the development of successive components utilizing reversible rationale entryways is very perplexing than that of combinational circuits. In this paper, we have confirmed a portion of the reversible doors both utilizing Cadence Virtuoso and H-Spice devices, we have additionally planned and mimicked reversible rationale based consecutive components, Consider D lock, D flip-flop, T flip-flop, and RS flip- lemon in terms of normal power, garbage outcomes, and the quantity of consistent data sources.

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )

Volume 5- Issue 1, Paper 36 January 2022

Reversible rationale doors are especially sought out for the future figuring degrees of progress as they are known to make zero power spread under wonderful conditions [5]. Reversible circuits hold guarantee in state-of-the-art enrolling advancements like low power VLSI, significant figuring, nanotechnology, optical dealing with, and so forth

Reversible rationale entryways require solid commitments for reconfiguration of section cutoff points and trash yields that assistance in keeping reversibility. By differentiating the various limits, it is possible to understand a singular entryway quality. Through this a circuit's direct can be researched [9]. The key aim of this paper is by differentiating the undeniable level calculation doors which are used in the circuits. By then the trash yield has been assessed. In this paper a review has been taken of significant level calculation doors and correlation has been finished with its examples. An unmistakable perspective on overview subtleties has been given in a relative table.

In light of its less warm scattering ascribes, reversible doors are generating appeal in the new past. The reversible reasoning doors aren't precisely the same as ordinary reasoning doors. However, in reversible reasoning doors, there could be no internal trading of signs and in this manner the glow dispersal can be restricted. Furthermore, reversible circuits have no dormant drawback. The majority of reversible rationale entryways distribute a lot of waste yields, which takes up a lot of space. [6].

Space may be conserved and the accuracy of the outcome can be maintained by effectively using these garbage yields. Recently, a reversible rationale door known as KISAN was designed, which effectively utilizes the waste yield. Furthermore, these doors were installed in a unique organization circuit in conjunction with the Wireless Sensor Network environment, and the efficacy of each reversible entryway's outcome was validated.

## III. Survey about Reversible Logic

An option is to utilize rationale activities that don't delete data. These are called reversible rationale activities, and on a basic level they can scatter subjectively little hotness [7]. As the energy disseminated per irreversible rationale activity moves toward the essential furthest reaches of ln 2 x kT, the utilization of reversible tasks is probably going to turn out to be more alluring [4]. On the off chance that latest things proceed with this ought to happen at some point in the 2010 to 2020 time period. Assuming that we are to diminish energy scattering per rationale activity beneath ln 2 x kT we will be compelled to utilize reversible rationale [2].

Nanotechnology should allow us to construct mole amounts of rationale components. Except if energy scattering per rationale activity can be diminished beneath kT, the crude expense of power may well demonstrate restrictive and the framework may rapidly overheat.

Indeed, even today the utilization of reversible rationale activities can be a valuable heuristic in the plan of frameworks that utilization very little power. Fig:2 illustrates the block diagram of reversible logic. To accomplish a totally reversible framework (which deletes no

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )
Volume 5- Issue 1, Paper 36 January 2022

pieces by any stretch of the imagination) is extremely challenging. As we permit an ever-increasing number of pieces to be eradicated during typical framework activity, it becomes simpler and more straightforward to plan the framework [3]. The present frameworks eradicate a cycle for each rationale activity they perform and are exceptionally dissipative. Frameworks that play out certain activities in a reversible manner can disperse less energy and might demonstrate serious (especially in specialty applications) today. There are two significant, firmly related kinds of reversibility that are quite compelling forthis reason:

- actual reversibility
- intelligent reversibility.


***Fig:2 Block diagram of Reversible logic***

An interaction is supposed to be truly reversible assuming it brings about no expansion in actual entropy; it is isentropic.

There is a style of circuit configuration in a perfect world displaying this property thatis alluded to as charge recuperation rationale, adiabatic circuits, or adiabatic figuring (see Adiabatic cycle). Albeit by and by no nonstationary actual cycle can be by and large truly reversible or isentropic, there is no known breaking point to the closeness with which we can move toward wonderful reversibility, in frameworks that are adequately all around segregated from communications with obscure outer conditions, when the laws of material science portraying the framework's development are exactly known. The XOR entryway represents the Exclusive-OR door. This entryway is an extraordinary kind of door utilized in various sorts of computational circuits. There are two unique doors, Ex-OR and Ex-NOR, in addition to the AND, OR, NOT, NAND, and NOR entryways. These doors aren't necessary on their own; instead, they're constructed by combining them with other logic doors. Their Boolean result work is large enough to be called a completerationale entranceway. The crossover doors are the XOR and XNOR entryways.

The 2-info OR door is otherwise called the Inclusive-OR entryway since when the two data sources An and B are set to 1, the result comes out 1(high). The logical yield "1" is obtained in the Ex-OR capacity only when either A="1" or B="1," but not both atthe same time. Just, the result of the XOR entryway is high (1) just when both the data sources are unique in relation to one another. The plus (+) sign inside the circle is utilized as the Boolean articulation of the XOR door. Thus, the image of the XOR door is ⊕. This Ex-OR image additionally characterizes the "immediate number of sub-objects" articulation.

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )
Volume 5- Issue 1, Paper 36 January 2022

## IV. KISAN GATE

This KISAN entrance is a 4X4 reversible door. It simultaneously performs the functions of a half snake and a half subtractor[10]. There is just one garbage yield. The square graph of the KISAN entrance is addressed in Figure 1. It contains information in the form of A, B, C, and D, as well as result bounds in the form of P, Q, R, and S. The block diagram of the KISAN gate is shown in

Figure 3.

P=A

Q= A^B

R= AB+C

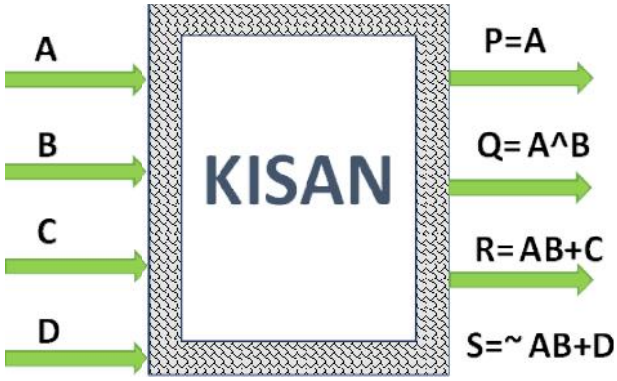
S= ~AB+D

.

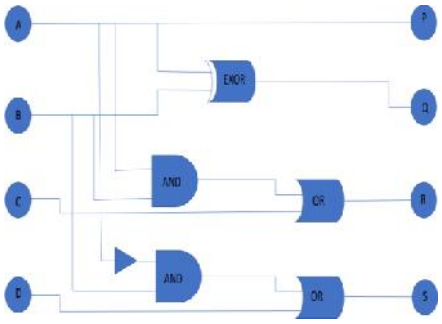
**Fig**:3 KISAN gate

Fig - 3 addresses the development ofKISAN door and Table - 1 addresses realitytable of KISAN entryway with different types of contribution for the information boundaries A, B and C.

The most important components for storing data are locks and flip-flops. The tiniest piece of data may be stored in a single lock or flip-failure. The main difference betweenlocks and flip-




flops is that hooks [11] contributions have an ongoing influence on



Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )

Volume 5- Issue 1, Paper 36 January 2022

their outputs as long as the empower signal is expressed. The internal structure of the KISAN gate is shown in Figure 4. At the end of the day, when people are empowered, their substance shifts quickly as their bits of input shift.

***FIG:4 Internal structure of KISAN gate***

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| A | B | C | D | P | Q | R | S |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

***Table:1 Truth table of KISAN gate***

After the assessment of test of reversible entryways, the experiences revealed that the majority of the entryways going under 4X4 and 3X3 entryway sizefragment. Under 4X4, 5X5 and 6X6 sections a model doorway has been givenfor each in the In future, if we have the options of merging the garbage yields, it would achieve imperative effects [8]. Most of the entryways are useful in arranging the circuits like full viper, convey skip snake, BCD snake, subtractor, Vedic multiplier, reversible multiplier, ALU, encoder, decoder, code converters, back-peddles, shift registers, counters, testing circuits, comparator, Wallace multiplier, grow convey snake etc.,[12]. Table 2 shows the close to blueprint of trial of raised levelestimation entryways close by specific guidelines. The principles that have been considered here are given under:

- Size of the door

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )
Volume 5- Issue 1, Paper 36 January 2022

- Trash Output
- Condition
- Significant Cost
- Circuit Design and
- Some more broad data

Reversible circuits are planned by utilizing the reversible rationale doors as it were. There are many circuits of 1-cycle full viper and subtractor plan [12]. Here two circuits are plan of full snake and subtractor Using 4 and 8 reversible rationale entryways and in this we can material alter only when the empowersignal is increasing or lowering. Normally, the controlling clock signal is this empower signal. Regardless matter whether the information changes, the flip-flop contentremains unchanged after the rising or lowering edge of the clock.

### *V. Reversible gates analyzation forlow power dissipation*

plan our circuit in the particulars of reversible rationale doors yet utilizing pass semiconductor and CMOS. A. 1-digit full snake and subtractor: In fig.9, 1-cycle reversible full-viper and subtractor [13] utilizing the 3 Feynman entryways, 2 TR doors, 1 Fredkin door and 2 Peres entryways to plan the circuit. Also, the control input is given to the switch in the middle of snake andsubtractor. On the off chance that gave control input is 1, expansion is accomplish and on the off chance thatthat is 0, deduction is achieve.[14].

Reversible rationale entryways areutilized in the security framework, expanding inordinate power usefulness, rate and affecting, less energy wastage and so forth [15] It incorporates a portionof the areas like plan of low power advanced circuit, field programmabledoor exhibits in CMOS, low powercircuit plans, nano innovation and the optical figuring and so on

### VI. Implementation of KISAN gate in Cryptography

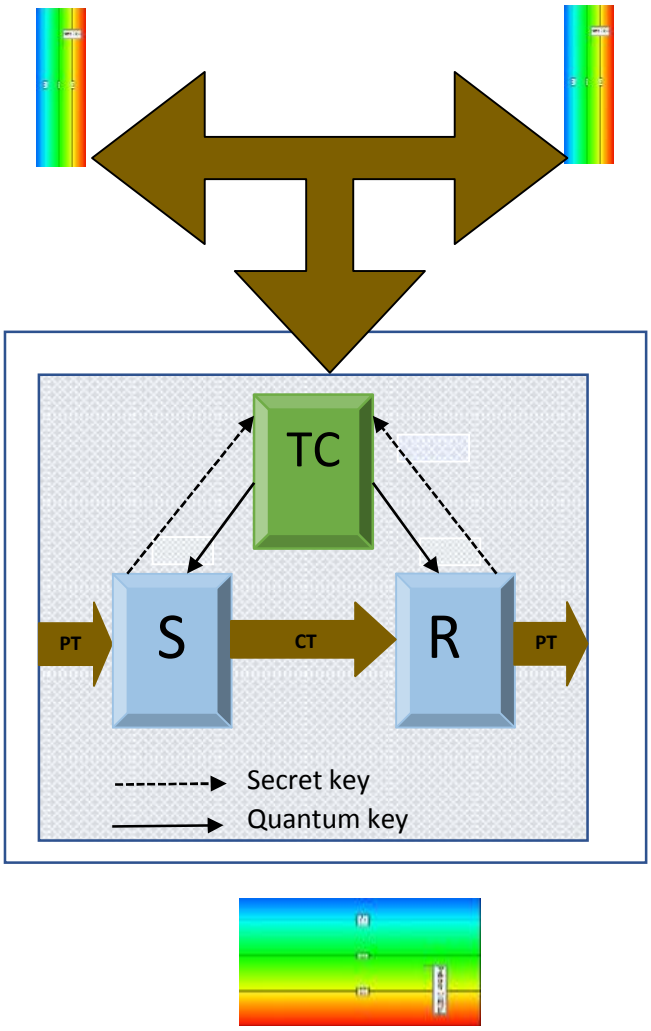
Cryptography today is heavily based on numerical hypothesis and software engineering practice; cryptographic computations are designed around computational hardness assumptions, making them tough to crack in real life by any adversary. While it is theoretically possible to break into a well-designed framework, it is impossible to do so in practice. Such plans are referred to as "computationally secure" if they are well-planned; hypothetical breakthroughs (e.g., improvements in whole number factorization operations) and faster calculating innovation need that these plans be rethought and, if necessary, updated on a regular basis. Data supposedly secure plans, such as the one-time cushion, that can't beproven to make back the initial expenditure with endless registering power, are much more difficult to apply effectively.

The implementation of the KISAN signal in a cryptographic context is shown in Figure 5. Although a message or set of messages might have a different key than others, symmetric-key cryptosystems employ the same key for encryption and decryption. The key management

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )



required to utilize symmetric cyphers safely is a big drawback. Each individual pair of communicating parties should, ideally, share a different key, as well as perhaps a different ciphertext for each ciphertextsent. The number of keys requiredgrows in direct proportion to the number of network participants, necessitating complicated key management techniques to keep themall consistent and hidden.




KISAN signal

***Fig:5 KISAN signal inCryptographic environment***

***This execution does thinks often about in security as well as it stays away from the information misfortune. This is accomplished by utilizing the trash yield in effective way. Figure 9 shows the consolidation of remote sensor network climate alongside

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )
Volume 5- Issue 1, Paper 36 January 2022

significant key appropriation convention utilizing KISAN entryway to get secure and lossless transmission. The TC and a portion of the QKDPs synchronize their polarization basesusing a pre-shared secret key in the proposed approach. The pre-shared secretkey and a discretionary string are used to create significant key with the aid of another key constructed conference key during the significant key distribution. Whether or whether an undefined secret key is retransmitted, the receiver will not get equivalent polarization qubits. The 4x4KISAN door is performed in the circuit's confided in concentration (TC) to provide a lossless and secure transmission between the shipper and the recipient. With the help of this 4x4 KISAN door, the polarization light beams that were used to convert the bundles into qubits were completed. It will also offer instructions on how to convert a plain message to a figure message. As aresult, in the WSN environment, a protectedand lossless transmission has been enhanced.

Factors: 4 ○ Horizontal ◉ Vertical

| | A [Numeric] | B [Numeric] | C [Numeric] | D [Numeric] |
|---|---|---|---|---|
| Name | A | B | C | D |
| Units | 1 | -1 | -1 | 1 |
| Type | Numeric | Numeric | Numeric | Numeric |
| Low | -1 | -1 | -1 | -1 |
| High | 1 | 1 | 1 | 1 |

***Fig:6 Regular 2-level factorial design ofKISAN gate***

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal ( ISSN : 2581 - 611X )



| S.No | Name of the Gate | Size of the Gate | Garbage Output | Equation | Q.C | | General information |
|---|---|---|---|---|---|---|---|
| 1. | Feynman | 2 | 1 | P=A Q=A^B | 1 | Full-adder, Comparator | Also called controlled NOT gate. It acts as a buffer (If control input is logic Zero).It acts as an inverter (If control input is logic One). |
| 2. | Fredkin | 3 | 1 | P=A<br>Q=~AB^AC<br>R=~AC^AB | 5 | Full-adder, AND gate, OR gate, SR-Flip flop, D- Flip flop, shift register. | It is also called controlled swap gate. Energy consumption is equal to 18mw. |
| 3. | Toffoli | 3 | 2 | P=A Q=B<br>R=AB^C | 5 | Full-adder | It is also called controlled-controlled NOT gate (CCNOT). |
| 4. | TS-III | 3 | 2 | P=A Q=B<br>R=A^B^C | 2 | Comparator, Adder<br>Multiplie | - |
| 5. | SRK | 3 | 1 | P = ~A<br>Q = A^B^C R = ~AC^AB | 4 | - | - |
| 6. | MPG | 3 | 1 | P = A<br>Q = A^B<br>R = A~B^C | - | SR Flip-flop | - |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7. | SAM | 3 | 1 | P = ~A<br>Q = ~AB^A~C | 4 | SR Flip – flop D latch | - |
| | | | | R = ~AC^AB | | JK latch | |
| 8. | DINV | 3 | 0 | P = ~A. B<br>Q = A.B<br>R = A.C | - | Decoder (4:16) & (5:32) | - |
| 9. | RG2 | 3 | 1 | P = ~A~B^C<br>Q = ~A^~B<br>R = A | 5 | Single precision | It is used for copy operation. It is used to implement OR, AND, XOR&NOT operation. |
| 10. | M | 3 | 1 | P =A,Q= ~(A+B) R = A~B^C | - | Comparator | - |
| 11. | L | 3 | 2 | P =A,Q = B, R = ~(A+B) ^C | - | Comparator | - |

***Table:2 Reversible gate analyzation***

## VII. CONCLUSIONS AND FUTURE ENHANCEMENT

There are 25 reversible rationale doors are thought about and numerous boundaries have been investigated. Trashresults of the reversible doors are taken intogenuine thought for planning furthercircuits. As the choice of specific reversible door assumes a significant part in electroniccircuit, a wide assortment of decisions has been given in this paper.

In this work, the sign of KISAN door has been executed helpfully in cryptographic procedure. These entryways are exceptionally a reversible rationale gate with low trash yield esteemed one. Indeed, even this trash result could be effectively utilized for lossless transmission. In the future, this higher recurrence signal doorwill be used in conjunction with the Significant Key Distribution Protocol to achieve a lossless exchange between a shipper

and a recipient in a Wireless SensorNetwork. The conventional two-level factorial design of the KISAN gate is shown in Figure 6. In this climate, this has been done by enveloping KISAN signalswith Trusted Center. These were designed and implemented with the help of Tanner programming, and their presentation was approximated with the help of various limits.

## XII. REFERENCES

S. Ahmed, N. Javaid, S. H. Bou, A. Javai, M. A. Khan, Z. A. Khan, "SIGNIFICANT CRYPTOGRAPHY USING VARIOUS REVERSIBLESIGNIFICANT LOGIC GATES IN WSNS", 2019, vol.13 ISSN 6, pp:806- 815. MOJTABA NOORALLAHZADEH,
MOHAMMED MOSLEH, "Efficient designs of reversible latches with low significant cost", IET CIRCUITS DEVICES SYSTEM, 2019, vol.13 ISS 6, pp:806-815.

Anamika, Rockey Bhardwaj Reversible logic gates and its performances IEEE Xplore Compliant - Part Number: CFP18J06-ART,ISBN:978–1–5386–0807–4

[4]J W Bruce, M A Thronton, L Shivakumaraiah, P S Kokate and X Li, "Efficient adder circuit based on a reversible logic gate", on VLSI., 2002.

L. Benini, E. Macii and G. De Micheli, "Designing Low Power Circuits: Practical Recipes" in IEEE Circuit and System Magazine, First Quarter, vol. 1, no. 1, pp. 6-25, 2001.

R. Landauer, "Irreversibility and heatgeneration in the computing process", IBM
J. Res. Develop., vol. 5, no. 3, pp. 183-191,
Jul. 1961

Kim Chulwoo and Kang Sung-Mo(Steve), "A Low-. Swing Clock Double- Edge Triggered Flip-Flop", IEEE J. of Solid-State Circuits, vol. 37, no. 5, May 2002.

E. Fredkin and T. Toffoli, "Conservativelogic", Int. J. Theor. Phys., vol. 21, no. 3/4, pp. 219-253, 1982.

[9]V.Sathya, Dr. Sridhar Chandrasekar, Dr.V.Vani, Kirankumar Manivannan,"SECURE COMMUNICATION WITHQKDP IN WSN USING REVERSIBLE
LOGIC GATES". International e - Conference on Cutting edge technologies inelectrical, communication, embedded system and soft computing techniques (ICECES'20), 2020.

[10]Kiran Kumar Manivannan, Dr.Shanthi, "Accomplishment of Reversible Logic Gates in WSN Environment by Patternization", Wireless PersonalCommunications, Pages 1-19, 2021.

[11]V.Sathya, S.Murali "SURVEY ON WIRELESS SENSOR NETWORK BASED SECURITY INTRUSION
DETECTION SYSTEM" InternationalJournal of Computer Science Engineering and Technology, Pages8-14, 2018

[12]V Sathya, S.Kannan, "RECOGNITIONAND PROTECTION OF BGP ROUTING TRANSGRESSION ACROSS TRUST AWARE ROUTING IN WIRELESS
SENSOR NETWORKS", Karpagam Jcs Vol. 12 Issue 3 Mar. - Apr. 2018

J. Suriya M. Kirankumar, A.P.Prabhakaran, "Reconstruction of Reversible gates with high performance and low power using 250nm technology in EDAtools", South Asian Journal of Research in Engineering Science and Technology,
Vol1,issue-4

DILIP P. VASUDEVAN et.al,"Reversible logic design with online testability", IEEE Transactions on Instruments and Measurements, vol.55, No.2, 2006.

Gaur, H. M., Singh, A. K., & Ghanekar, U. (2018) Testable design of reversible circuits using parity preservinggates. IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, 35(4), 56–64.
https://doi.org/10.1109/MDAT.2017.2771202