Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

Design of 16-bit Low power SRAM in 180nm CMOS technology

Shubham Santosh Kadam , Piyush Bhatasana
Department of Electronics and Communication Engineering
Institute of Technology, Nirma University
Ahmedabad, India

***Abstract*— The design and implementation of a 16-bit low-power SRAM are presented in this study. The conventional 6T SRAM and 8T SRAM in 16-bit configuration are implemented and compared with 16-bit low-power SRAM. The comparative analysis of power consumption is done for three different SRAM configurations. The various circuitry used in-memory architecture are described. Low power SRAM which is based on Multi-threshold CMOS technology shows a 45.3% reduction in power consumption for the read cycle and a 43.4% reduction in power consumption for the write cycle. The 16-bit memory architectures are implemented using a 180nm node CMOS process technology in the Ltspice tool.**

Keywords— SRAM, CMOS, Low power, Sense Amplifier.

I. INTRODUCTION

The Data is stored in memory cells created from MOS transistors on an integrated circuit in modern computers, which is implemented as a semiconductor memory. With the advancement in the semiconductor electronic industry, the technology node is shrinking and the demand for battery backup is also increasing. Static random access memory (SRAM) is a volatile memory. SRAM does not need periodic refreshing as in the case of Dynamic random access memory. SRAM has more speed as compared to DRAM.SRAM is used as cache memory in computers. SRAM cells have leakage power consumption. To minimize the leakage power, the multi-threshold technique (MTCMOS) is used in low-power SRAM[1].

II. MEMORY ARCHITECTURE

The organization for Random access memory is shown in Figure 1. It is called random access memory because the memory locations can be accessed in random order independent of their physical location, for reading and writing operations. Both a row decoder and a column decoder are used to access specific data, and by combining the two, the desired storage cell can be accessed.

A. Pre-charge circuit

In the read operation, the pre-charge circuitry is used to charge the bit lines to VDD[2]. The circuitry is made using PMOS transistors. A signal phi is applied to turn on the circuit. After pre-charging the bit lines the word line is made high. One of the bit lines remains high and the other bit line voltage starts falling. This change in potential is sensed by the sense amplifier. The pre-charge circuitry is shown in figure 2.

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

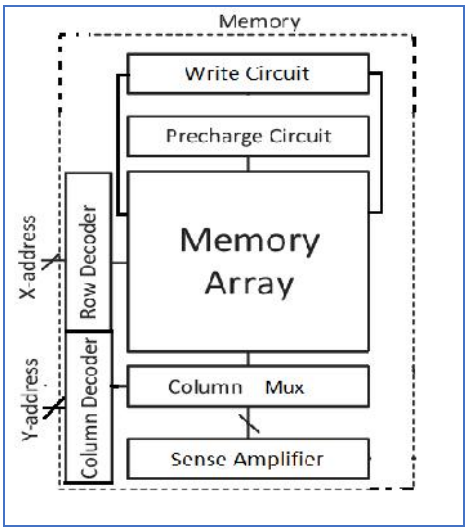


Fig. 1. Memory Architecture

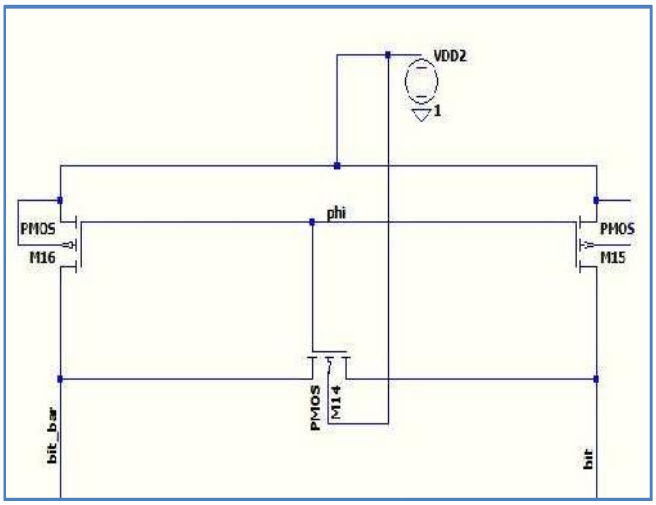


Fig. 2. Pre-charge circuit

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

B. Write circuit

The write circuit is used to write data to SRAM. During a write operation, the write enable signal (WE) and word lines are made HIGH while the pre-charge enable signal is made LOW[3]. The sense amplifier is disabled by making sense enable signal of the sense amplifier to HIGH. The data(D) to be written into the cell is supplied into the bit lines, resulting in the output of the data and its complement. The circuit for a write operation is shown in figure 3.

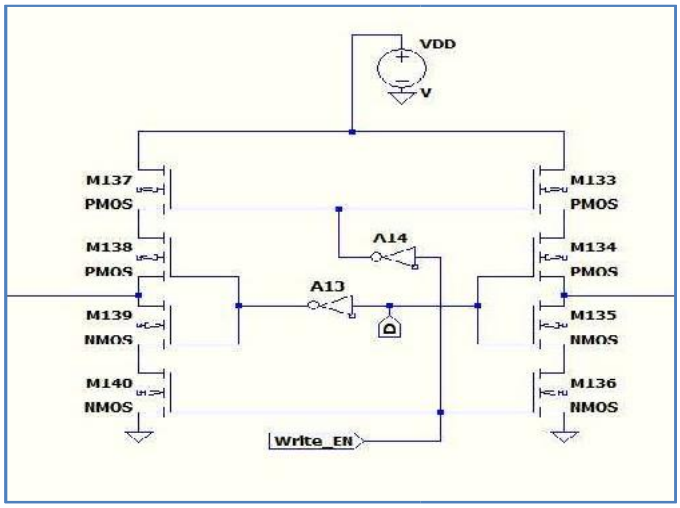


Fig. 3. Write circuit

C. Column Multiplexer

The column multiplexer is used to select columns in the memory array for reading or writing operations. The input of column multiplexer are bit lines and the output is connected to a common-sense amplifier. Instead of using a sense amplifier for every column, by using column multiplexer only one sense amplifier is required. Thus reducing power consumption and hardware as well. The Circuit for column multiplexer is shown in figure 4.

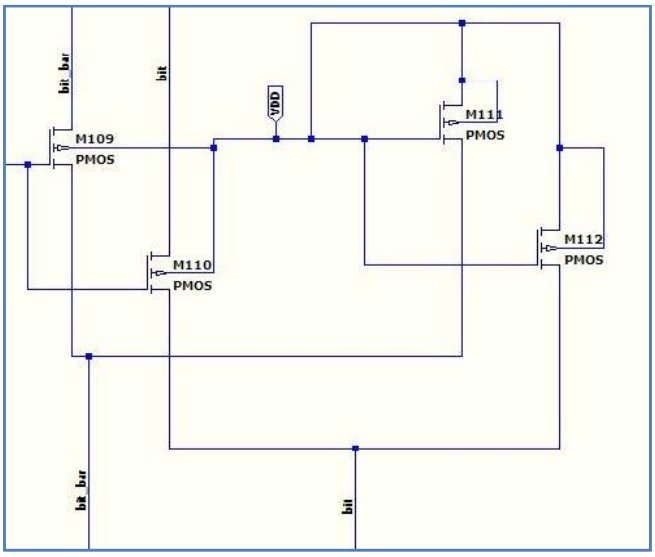


Fig. 4. Column multiplexer

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

D. Decoder

There are two decoders used in the memory architecture. Row decoder to select rows. The output of the row decoder is connected to word lines. Column decoder is used to select columns. The column decoder's output is connected to the column multiplexer. The circuit for the decoder is shown in figure 5.

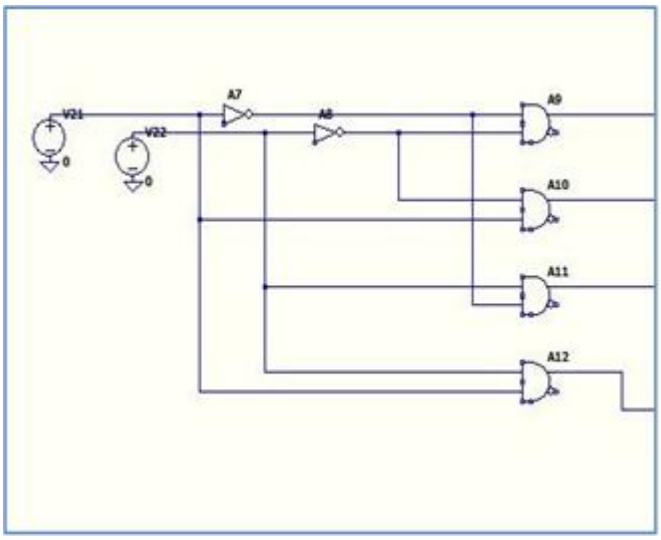


Fig. 5. 2:4 Decoder

E. Sense Amplifier

Latch type sense amplifiers are used to read the contents of memory. Two inverters are connected in a cross-coupled fashion to provide positive feedback. The sense enable signal turns on the amplifier and starts the sensing operation. Depending on the polarity of the voltage difference between the bit and bit bar lines, the sense amplifier will flip to 0 or 1[3]. The circuit for the sense amplifier is shown in figure 6.

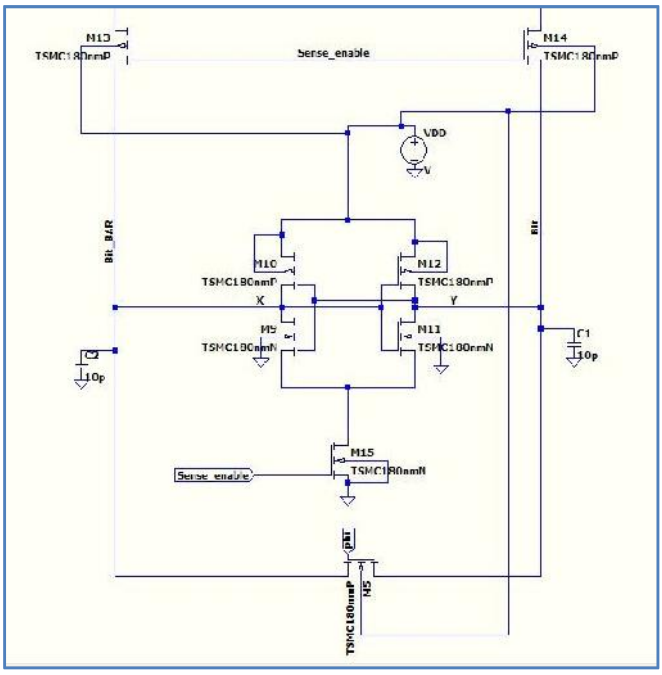
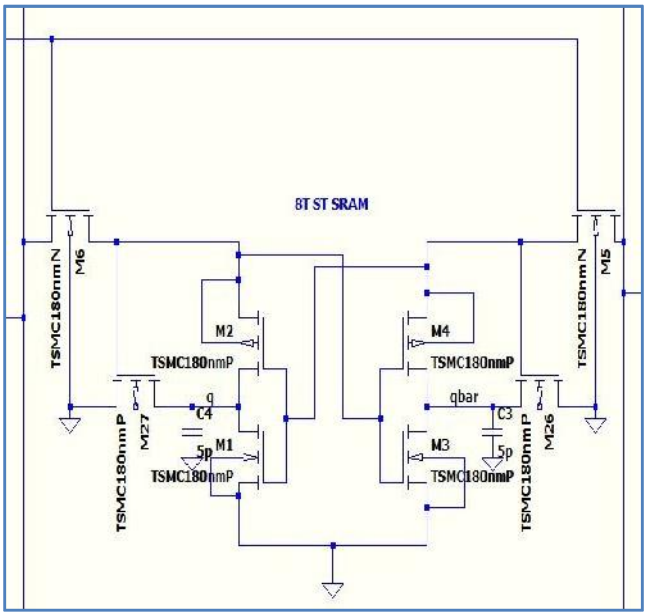


Fig. 6. Latch based sense amplifier

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022



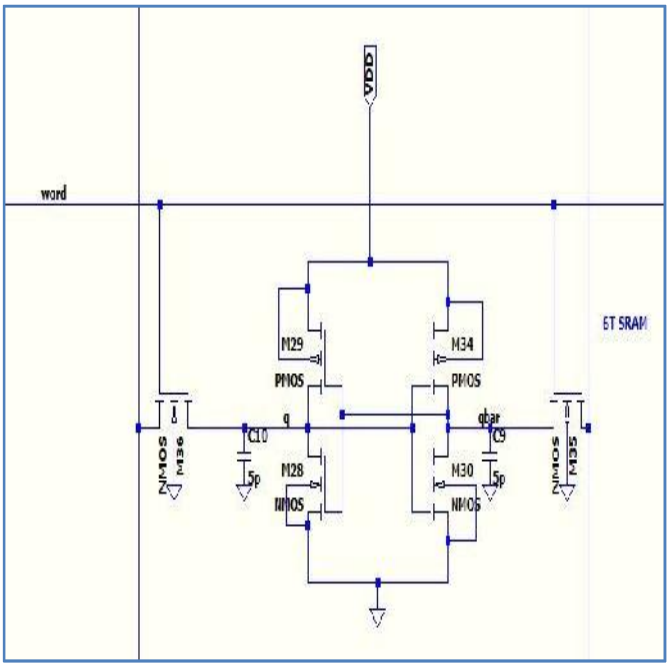
F. SRAM cell

The three different configurations presented in this paper are as follows:

1) 6T SRAM

The conventional 6-T SRAM cell employs two CMOS inverters that are cross-coupled[4]. As indicated in Figure 7, two NMOS are employed as access transistors. The word line is connected to the access transistors. The memory element is the inverter, which holds the data bit within the cell as long as the power supply is turned on.

Fig. 7. 6T SRAM



2) 8T SRAM

The proposed design aims at making basic inverter pair of SRAM cells efficient for low voltage operations. The circuit diagram for 8T SRAM is as shown in figure 8. In the cell shown in Fig.8, PMOS transistors are used as drivers and NMOS

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

transistors are used as pass transistors to access the cell. At low voltages, SRAM cell stability is of major concern. 8T ST SRAM cell is used to improve read stability at the expense of speed as PMOS transistors are used as drivers for the cell[5].

3) Low power SRAM

In this design, transistors having multiple threshold voltages are used to decrease power consumption. A low threshold voltage (Vt) transistor will have higher static power leakage but switching will be faster. A High threshold voltage transistor will switch slower but will reduce static power leakage. These High Vt and Low Vt transistors are turned ON and are OFF by the decoder signal. Static leakage power will be reduced by a huge amount by these sleep transistors when the SRAM cell is in an idle state[2]. The Low power SRAM circuit is shown in figure 9.

Fig. 8. 8T SRAM

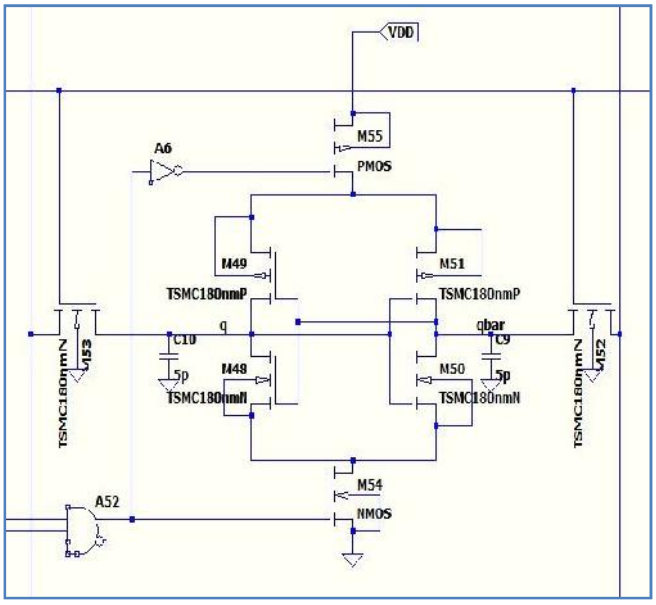


Fig. 9. Low power SRAM

III. SIMULATION AND RESULTS

A. Write operation

Write operation simulation in Ltspice is shown in figure 10. During a write operation, the write enable(write_en) signal is made high. The (sense_enable) signal of sense amplifier is made low. Pre-charge circuitry is turned OFF by making the pre-charge enable signal (phi) signal high[6]. The data is written by 'd' signal and the output is obtained at the q and qbar terminal.

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

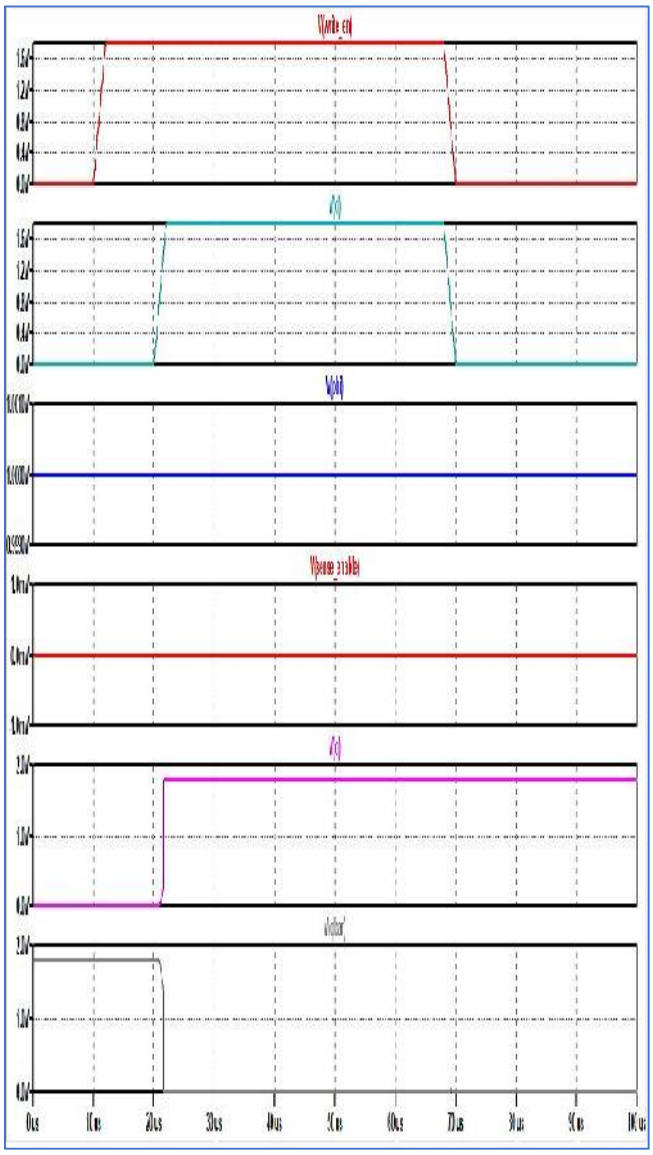


Fig. 10. Write operation

B. Read operation

Read operation simulation is shown in figure 11. To read the data from the memory, a sense amplifier is used. The nodes x and y will indicate the value stored in the SRAM cell. The Write enable(write_enable) and the data signal(d) is made low during the read operation. the corresponding row is selected by enabling the word line (word) to read a particular word from the SRAM array. The sense amplifier is enabled by the signal named (sense_enable)[7].

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

Table. 1. Average power consumption of different SRAM configurations

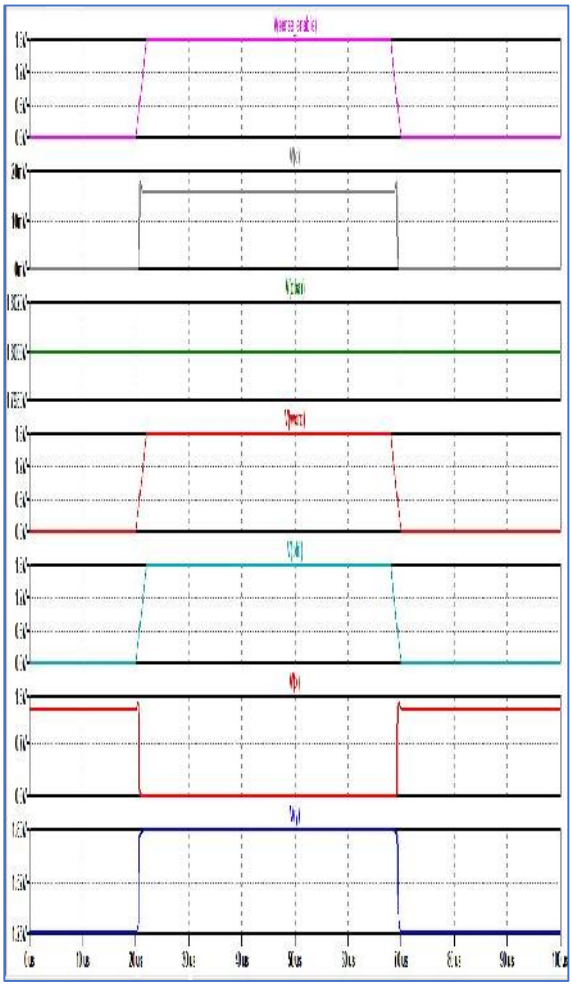
Parameters		Conventional6T SRAM	8T SRAM	Low power SRAM
Averagepower	Read cycle	893.71uW	493.85uW	488.79uW
	Write cycle	1.45mW	835.71uW	822.5uW

Fig. 11. Read operation

Table 2.. Read and Write delay

Parameters		Conventional6T SRAM	8T SRAM	Low power SRAM
Delay	Read cycle	1.97us	1.88us	2.02us
	Write cycle	2.5us	5us	2us

The 4x4 SRAM architecture is shown in figure 12.



Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

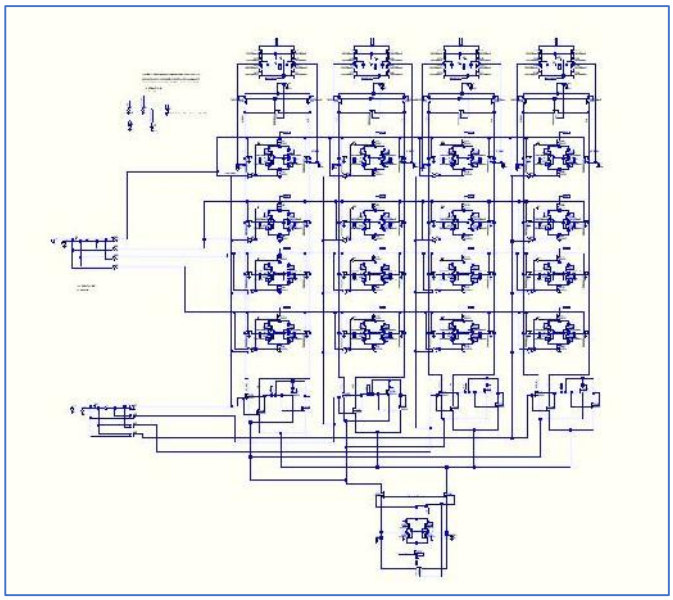


Fig 12. 4x4 SRAM

The average power is calculated for one clock cycle, which can contain one write or one read operation[4]. Figure 13 shows the average power consumed by a conventional 6T SRAM cell, an 8T SRAM cell, and a low-power SRAM cell.

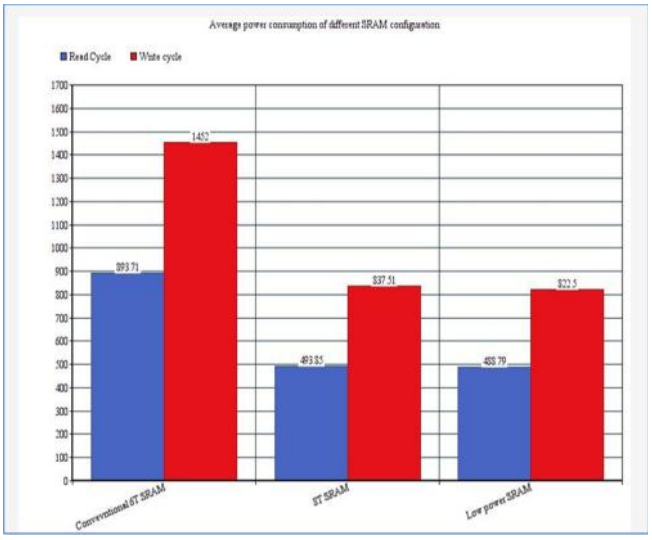


Fig. 13. Avg. Power Consumption Comparison between different SRAM configurations

CONCLUSION

In this paper, 16-bit SRAM cell using different configurations is designed and analyzed in 180nm CMOS technology. Based on the above-simulated results, Low power SRAM cells have the lowest power consumption as compared to 6T and 8T SRAM cells. Also, read and write operation is performed. Low power SRAM shows a reduction in power consumption for the read cycle and write cycle. In comparison with 6T SRAM, the low-power SRAM is 20% faster. The only drawback is

Journal of Current Research in Engineering and Science
Bi-Annual Online Journal (ISSN : 2581 - 611X)
Volume 5- Issue 2, Paper 5 August 2022

area overhead due to an increase in the number of transistors.

REFERENCES

[1] F. Moradi and J. K. Madsen, "Improved read and write margins using a novel 8T-SRAM cell," *IEEE/IFIP Int. Conf. VLSI Syst. VLSI-SoC*, vol. 2015, no. January, 2015, doi: 10.1109/VLSI-SoC.2014.7004186.

[2] P. Chodankar, I. Suryavanshi, and A. Gangad, "Low power SRAM design using independent gate FinFET at 30nm technology," *2014 1st Int. Conf. Comput. Syst. Commun. ICCSC 2014*, no. December, pp. 52–56, 2003, doi: 10.1109/COMPSC.2014.7032620.

[3] S. Birla, N. K. Shukla, D. Mukherjee, and R. K. Singh, "Leakage current reduction in 6t single cell SRAM at90 nm technology," *ACE 2010 - 2010 Int. Conf. Adv. Comput. Eng.*, no. June, pp. 292–294, 2010, doi: 10.1109/ACE.2010.42.

[4] A. Bhaskar, "Design and analysis of low power SRAM cells," *2017 Innov. Power Adv. Comput. Technol. i-PACT 2017*, vol. 2017-Janua, pp. 1–5, 2017, doi: 10.1109/IPACT.2017.8244888.

[5] P. L. Achankunju, S. K S, and M. K. James, "Design and Read Stabilityanalysis of 8T Schmitt Trigger Based Sram," *ICTACT J. Microelectron.*, vol. 02, no. 04, pp. 323–328, 2017, doi: 10.21917/ijme.2017.0056.

[6] P. Sharma and M. S. Hashmi, "A novel design of a Dual Functionality Read-Write driver for SRAM," *Int. Syst. Chip Conf.*, vol. 0, pp. 280–285, 2016, doi: 10.1109/SOCC.2016.7905487.

[7] R. Sandeep, N. T. Deshpande, and A. R. Aswatha, "Design and analysis of a new loadless 4T SRAM cell in deep submicron CMOS technologies," *2009 2nd Int. Conf. Emerg. Trends Eng. Technol. ICETET 2009*, no. January, pp. 155–161, 2009, doi: 10.1109/ICETET.2009.67.