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A Survey on On–Chip Communication and Network – on – Chip Architectures

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Abstract – The enormous growth of transistors on the Chip are increased, it leads to the growth of the System-on-Chip (SoC). The SoC design has important features like speed, capacity, size, power consumption and cost are less. The System-on-Chip (SoC) features has to grow for the further signal integration, Synchronization and power dissipation. To overcome this problem of System-on-Chip the Network-on-Chip (NoC) has been proposed. The Network-on-Chip (NoC) is promising solution for power, performance demands and scalability to overcome the problems of the System-on-Chip(SoC) of the basic architecture.

This paper is basically the review of Network-on-Chip(NoC) and the architectures of the NoC. The On-Chip Communication and Network-on-Chip Architectures are tabulated. The On-Chip Communication architectures are the Future Multiprocessor System-on-Chip (MPSoC's) for the Chip development of (Tens to Hundreds) of components on the chip. The Characteristics of Network-on-Chip are Network Topology, Switching Strategies, Routing Algorithm, Flow Control, Clocking Schemes, Quality of Service.

Keywords: Network-on-Chip, NoC Architecture, System-on-Chip, Multi-Processor System-on-Chip.

I. INTRODUCTION

The idea of using the Network-on-Chip (NoCs) on the On-Chip Communication Fabrics is developed for the future Multiprocessor Systems-on-Chip (MPSoCs).The NoC are used to scale down the network and apply them to the System-on-Chip (SoC). The NoC uses packets to route data from the source to the destination, through the switches (routers) and interconnection link (wires).

The two major factors that have growing the interest in NoCs. First, the electronic systems are becoming complex. In 1990's the SoC design consisted with handful of components e.g.: digital Signal processor(DSP), microprocessor, memory and interfaces. The SoC design is evolved into multiprocessor SoC design having tens to hundreds of components(e.g.-IBM's cell chip[1]).

Later, the complex systems will have hundreds of components operating in gigahertz (GHz) frequency. In that scenario, there is a need for scalable and Quality of Service(QoS) needs for the complex systems.

Secondly, the shrinking process technology into deep submicron (DSM) (i.e,below 90nm) wire delays due to inductive and capacitive coupling effects, synchronization failures. NoC's [2] improves the scalability of SoC and power efficiency of complex SoC of communication design system.

II. CHARACTERISTICS OF NETWORK-ON-CHIP

The design problems of the Network-on-Chip remains the same tradeoff Performance, Power, Cost, Area, Reliability to communication Fabric. The NoC are used to scale down the concepts of large scale Network and apply them to the Embedded SoC domain. The Network-on-Chip is defined as the working of the On-Chip Communication fabrics for future(MPSoCs). Unlike the Bus-based communication, the NoC uses packets to route the data from source to the destination through the network fabric. It uses switches and interconnection links, as switches works as router and links as wires.

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The characteristics of Network-on-Chip are the Network Topology, Switching Strategies, Routing Algorithm, Flow Control Schemes, Clocking Schemes and Quality of Service. The topology of an NoC specifies the physical organization of the interconnection network. It defines how nodes, switches, and links are connected to each other.

1. Network Topology :

Topologies for NoCs canbe classified into three broad categories direct networks, indirect networks, and irregular networks. These are described below.

i. Direct Networks :

In direct network topologies, each node has direct point-to-point links to a subset of other nodesin the system called neighboring nodes. The basic property of the direct network topology is that as the no. of nodes in the system increases, the total available communication bandwidth also increases. The direct network is trade-off between the connectivity and cost. In this topology is implemented using the orthogonal implementation, the links produce a displacement in single direction. The Examples of popular orthogonal direct networks include the n-dimensional mesh, torus, foldedtorus, hypercube, and octagon topologies.

ii. Indirect Topology :

In the indirect network topologies, each node is connected to an external switch, and switches have point-to-point links to other switches. The NI associated with each node connects to a port of a switch. One of the simplest indirect networks topology is a crossbar, where each PE node is connected to any other PE by traversing just a single switch. The Clos network and Benes are examples of a non-blocking network for Indirect Topology, which is expensive because it consists of several full crossbars. The SPIN NoC architecture is an example of an indirect network.

iii. Irregular Topology :

Irregular or ad hoc network topologies are usually a mix of shared bus, direct, and indirect network topology bandwidth as compared to traditional shared buses, and reduce the distance between nodes as compared to direct and indirect networks. Irregular topologies are typically customized for an application. The example of an Irregular Topology cluster-based hybrid topology which combines a mesh and a ring topology. Xpipes and Æthereal are two examples of NoC architectures thatallow irregular topologies.

2. Switching Strategies :

The NoC switching strategy explains how data flows through the routers in the network. Switching strategies are defined as the granularity of data transfer and is applied on the switching technique.The packet is further divided into multiple flits (flow control unit). A flit is defined as an elementary packet in which link flow control operations are performed, and is used as an essentially for synchronization unit between the routers. Each flit is made up of one or more Phits (physical units). A Phit is a unit of data that is transferred on a link in a single cycle.

The Switching Strategies are divided into two types, they are circuit switching and packet switching. These are described below.

1. Circuit Switching :

The transmission of data is reserved prior, and a physical path between the source to the destination to transfer the data. The physical path is defined as a series of links and routers, and the messages are sent to the receiver once the path reserved in the circuit. The message header flit traverses the network from source to the destination, reserving the links along the traversing way. The SOCBUS NoC architecture is implemented using the circuit switching. The advantage of circuit switching, by using the multiplex where multiple virtual links on a single physical link uses a virtual circuit switching reserves the physical link between routers. In virtual circuit switching, it creates virtual circuits that are used for the multiplexing on links. The virtual links are also called as (Virtual Channels (VCs)) where it can support a physical link depends on the buffers allocated to the links.

The two popular schemes are used for virtual circuit switching in Network-on-Chip are involved in which either allocating one buffer per virtual link , or allocating one buffer per link.

Allocating one buffer per virtual link :

In the first scheme of virtual circuit switching, the virtual circuit requires a buffer in each router when it passes through the network. In each router requires the number of buffers and is determined by Network-on- Chip based on how virtual circuits are spatially distributed. The MANGO NoC architecture uses a variant of this

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scheme.

Allocating one buffer per link :

In the second scheme of virtual circuit switching, the virtual circuit requires a time multiplexed with a single buffer per link. This is achieved by using time division multiplexing (TDM) to statically schedule the usage of links among virtual circuits, the Flits are typically buffered at the NIs and sent into the NoC according to the TDM schedule. Nostrum and Æthereal are examples of NoC architectures that use this scheme.

2. Packet Switching :

The packet switching is defined as the switching is done by the packets independently from the source to the receiver, along from the source to the receiver with different routes and different delays. The packet switching uses packets to transfer data. The packet switching is divided into popular schemes : 1.store and forward (SAF), 2. virtual cut through (VCT) and 3.wormhole (WH)switching.

In the store and forward switching technique , a packet is sent from one router to the next only if the receiving router has buffer space for the entire packet. It is commonly, not used in NoCs because of large buffer size requirements for this technique. This technique is used in the NoC architecture of Nostrum, it makes use of SAF switching (along with deflective routing).

In the Virtual Cut Through Switching technique, it reduces the router latency over SAF switching by transferring the first flit of the packet as soon as the space for the entire packet is available in the next router (instead of first waiting for the entire packet to be received and then ensuring that sufficient buffer space is available in the next router before initiating packet transfer). The buffering requirements for this scheme are same as that of SAF, and this technique is also not frequently used by the NoC's.

In Wormhole switching technique, the buffer requirements are reduced to one flit, instead of the entire packet. A flit from a packet is transferred to the receiving router , if the space for that flit is available in the router. By the distribution of packets among multiple routers results in blocking of links, which leads to the higher congestion than in the SAF and VCT. The WH Switching is also more susceptible to deadlocks than in the both SAF and VCT Switching, due to the dependencies between the links. The most NoC's architecture uses WH (Wormhole Switching) the example (e.g: SPIN or a combination of WH and virtual circuit switching ; e.g : MANGO , AEthereal).

3. Routing Algorithms :

The Routing algorithms are responsible for correctly and efficiently routing packets or circuits from the source to the destination. The choice of a routing algorithm depends on trade-off between several potentially conflicting metrics such as minimizing power required for routing, minimizing logic and routing tables to achieve a lower area footprint, increasing performanceby reducing delay and maximizing traffic utilization of the network, and improving robustnessto better adapt to changing traffic needs.

Routing schemes can broadly be classified into several categories such as static or dynamic routing, distributed or source routing, and minimal or non-minimal routing. The Routing decisions in an NoC architecture router can be either static (also called deterministic or oblivious) or dynamic (also called adaptive). In the static routing, the fixed paths are used to transfer data between a particular source and destination. This routing scheme does not take into account the current state of the network, and is unaware of the load on the routers and links when making routing decisions. The many advantages of the static routing is that it is easy to implement,since very little additional router logic is required.

The dynamic routing, the routing decisions are made according to the current state of the network, the considering factors such as availability and load on links. The dynamic routing is also called as adaptive routing behavior comes at the cost of additional resources that continuously monitor the state of the network and dynamically change routing paths. This also allows support for more traffic on the same NoC topology.

In the distributed routing, each packet carries the destination address and routing decisions are made in each router by looking up the destination addresses in a routing table or by executing a hardware function. In the Source routing, pre-computed routing tables are stored at a node 's (or PE 's) NI. When a source node transmits a data packet, the routing information is looked up at the source router (or NI) based on the destination address, and this information is added to the header of the packet.

A routing is minimal if the length of the routing path

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from the source to the destination is the shortest possible length between the two nodes. In minimal routing, the source does not start sending a packet if a minimal path isnot available. In contrast, a non-minimal routing scheme does not have such constraints, and can use longer paths if a minimal path is not available. By allowing non-minimal paths, the number of alternative paths is increased, which can be useful for avoiding congestion. Non-minimal routing can, however, have an undesirable overhead of additional power consumption in NoCs.

4. Flow Control :

The goal of the flow control is to allocate network resources for packets traversing an NoC. In the data link-layer level, when transmission errors occur, recovery from the error depends on the support provided by the flow control mechanism. if a corrupted packet needs to be retransmitted, the flow of packets from the sender must be stopped, and request signaling must be performed to reallocate buffer and bandwidth resources.

Most flow control techniques can manage link congestion, but not all schemes can (by themselves) reallocate all the resources required for retransmission when errors occur. The Flow control has divided into 2 categories in to Data link-layer ,Network and Transport layer Flow control.

i. Data Link-Layer Flow Control:

The commonly used flow control schemes at the data link layer in NoCs, such as STALL/GO, T-Error , and ACK/NACK. Each of these schemes offers different fault tolerance features with different power, performance, and area overheads.

ii. Network and Transport-Layer:

Flow control techniques are also implemented at the higher network and transport layers, where flows between the sender and receiver are handled. Techniques for flow control at the network and transport layers can be classified according to whether they require resource reservations or not.

5. Clocking Schemes :

The Clock distribution is defined as an important component for the modern synchronous digital system design because clock trees can consume a significant amount of the total power of a chip (over 30% in some cases). The large contribution of the total power consumed by the clock network is due to the fact that a clock signal needs to connect to every single flip-flop and latch in the system, for the system to function properly.

The NoCs, there are several different clocking schemes are available, such as fully synchronous, mesochronous, pleisochronous, and asynchronous. In the fully synchronous case, a single global clock is distributed to synchronize the entire chip. The clock signal arrives simultaneously at the local flip-flops of routers, nodes, and buffered links all over the chip. To overcome this problem, multiple clock domains are used. In the mesochronous case, local clocks are derived from a global clock thathas been distributed all across the chip. All synchronous modules in a mesochronous system use the same clock source, but the phase between clock signals in different modules may differ due to an unbalanced global clock network. The clocking in this case is not sensitive to clock skew. In the pleisochronous case, clock signals are produced locally. The local clock is almost at the same frequency as clocks produced elsewhere, causing a small frequency drift.

A globally asynchronous locally synchronous(GALS) scheme is an extension of this paradigm, where asynchronous communication protocols are used to communicate between locally clocked regions. This effectively eliminates the clock skew problem and exploits the advantages of both 459 synchronous and asynchronous systems. However, using an asynchronous protocol (such as handshaking on global wires) can degrade Performance because a signal must make a round trip for every signal transaction. One solutionis to use asynchronous pipelining which can improve throughput on long links.

6. Quality of Service :

QoS in NoCs refers to the level of commitment for packet delivery. The commitment can be correctness of the transfer, completion of the transaction, or bounds on performance. In most cases, QoS actually refers to bounds on performance (bandwidth, delay, and jitter) since correctness and completion are often the basic requirementsof on-chip packet transfers. Correctness is concerned with packet integrity (corruption-less) and in-order transfer of packets from the source to the intended destination. Different strategies at different levels of the protocol stack, such as error correction atthe data link layer or retransmission at the upper layers to guarantee packet integrity, and network or transport-layer protocols to ensure in-order packet delivery. Completion requires that packets are not dropped or lost when being transferred from the source to the intended destination. Completion also ensures that

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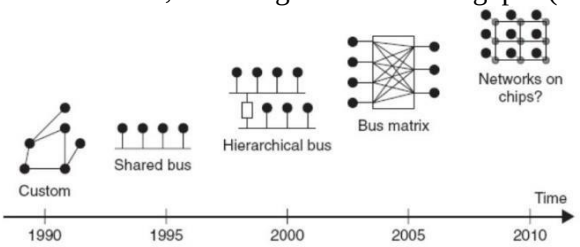
no deadlocks or livelock occur.

In terms of bounds on performance, QoS requirements can be classified into three basic categories: best effort (BE), guaranteed service (GS), and differentiated service. In BE, only the correctness and completion of communication is guaranteed and no other commitments canbe made. Packets are delivered as quickly as possible over a connectionless (i.e., packet switched) network, but worst case times cannot be guaranteed, and can be an order of magnitude worse than the average case.

A GS, such as guaranteed throughput (GT), makes a tangible guarantee on performance, in addition to the basic guarantees of correctness and completion for communication. GS is typically implemented using connection-oriented switching (i.e., virtual circuit switching). A differentiated service prioritizes communication according to different categories, and the NoC switches employ priority based scheduling andallocation policies. The signaling classis given the highest priority and the block data transfer the lowest priority. Unlike GS, the priority-based approaches can enable higher resource utilization, but do not provide strong guarantees.



III. ON – CHIP COMMUNICATION ARCHITECTURES

The electronic components are evolved as diodes,transistors and then as integrated circuits and later microprocessors and System-on-Chip(SoC).

A Single chip integrated circuits are commonly referred as System-on-Chip(SoC) consists of several complex heterogeneous components, such as programmable processors, dedicated(custom)hardware to perform Specific tasks, on-chip memories, I/O Interfaces.

The On-Chip Communication architecture is defined as that it serves the interconnection fabric for communication between these components. The Multiprocessor System-on-Chip(MPSoC) designs typically consist of multiple microprocessors, and ten to hundreds of components. The On-Chip communication architecture ensure that the multiple, co-existing data streams on the chip are correctly and reliably routed from the source components to the intended destinations.

The correctness, has to provide latency (or) Bandwidth guarantees to ensure that the application performance constraints are satisfied. The Latency guarantees implies that data unit traverse the communication architecture and reach its destination within finite time determined by Latency bound(e.g.: 20ns from source to the destination). Bandwidth guarantees implies, the group of data units must traverse a portion of the rate, as determined by the Bandwidth requirements(e.g:150 megabits/sec from source to destination). The fig-1 shows the evolutionary process of On-Chip Communication architectures[22].

Fig-1 : Evolution of On-Chip Communication Architectures

The Evolution of On-Chip Communication architectures are Custom, Shared bus, Hierarchical bus, Bus matrix, Network-on-Chip[23]. The custom architectures are an attempt to address the shortcomings of standard On-Chip communication architectures by utilizing new topologies and protocols to obtain improvements for common designgoals, such as performance and power. A Bus is a collection of Signals (wires)to which one or more IP components(which need to communicate with each other)are connected. Only one component can transfer data on the shared bus at any given timeshared bus architecture is not scalable to meet the demands of MPSoC applications.

Table-1:Advantages and Disadvantages of On-Chip Communication architectures.

On-Chip Communication Architectures	Advantages	Disadvantages
Custom (1990)	To address the short comings of Standard On-Chip Architecture by New Topologies and protocols	The Design Goals are not Improved.
Shared Bus (1995)	Many Contemporary MPSoC	Limits the Parallelism and achievable

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	designs use single shared bus based communication architecture.	performance in the System unsuitable for most of the MPSoC applications.
Hierarchical Bus (2000)	Hierarchical Buses are Interconnected using Bridge Components	The shared buses lower down the Hierarchy are operated allow frequencies to save power and high latency, low performance components.
Bus Matrix(2005)	Crossbar architecture connects processors on the left memories and peripherals on the right	It uses more wires and logic components to support high performance requirements, larger power consumption and area overhead.
Network-on-Chip (2005)	Network-on-Chip are Fully Scalable, Design Space is Larger	NoC based architecture and packet switching provide dynamic communication possibilities, which leads to versatility.

The basic building block of On-Chip Communication architecture is single shared bus, which consist of set of shared, parallel wires to which various components are connected. Only one bus can have control of the shared wires at any given time to perform data transfers. Many Contemporary MPSoC[24] designs use shared bus based communication architectures.

The Hierarchical shared bus architecture which consists of a hierarchy of buses interconnected using on right. it is a combination of shared bus and point- to-point interconnections. Each of this bus-based On- Chip Communication architecture is defined by its two major constituent's topology and protocol parameters[25].

IV. NETWORK – ON – CHIP ARCHITECTURE

The Network – on – Chip Architecture defines a Topology and set of protocols that typically determine schemes for Switching, Routing, interfacing, Clock distribution and Flow Control. The choice of Network – on – Chip architecture is determined by one or more design criteria, such as requirements for performance, Latency and Throughput , Power Consumption, Quality of Service, Reliability, Scalability and Implementation cost.

i. AEthereal :

It is developed by Philips is an Sychronous indirected Network (but also supports irregular topologies).uses WH Switching and can provide GT(Guaranteed Throughput) as well as BE(Best Effort) QoS(Quality of Service)[3].Virtual Circuit Switching is used to implement GT(Guaranteed Throughput)[4,5].

AEthereal Implements a Digital Video receiver and a high endconsumer TV Systems is compared to traditional interconnect Solutions[6,7].

ii. HERMES :

Developed at the Faculdade de Informatica PUCRS, Brazil, NoC is a direct network with a 2D Mesh topology, WH Switching, minimal XY Routing Algorithm. HERMES[9,10] is a connectionless, and it cannot provide any form of Bandwidth (or) Latency GS(Guaranteed Service).

iii. MANGO :

The MANGO Network (Message Passing Asynchronous Network-on-Chip Providing GS over open core protocol(OCP)[8] interfaces).

Developed at the Technical University of Denmark, is a clockless NoC that Provides BE as well as GS Services[11].

iv. NOSTRUM :

Developed at KTH in Stockholm is a Direct Network with a 2D Mesh Topology. NOSTRUM[12,13] makes use of Deflective Routing Scheme with SAF Switching and provides support for Switch load distribution, Guaranteed Bandwidth(GB) and Multicasting.GB is realized using looped containers are implemented by Virtual Circuits, using a TDM Mechanism referred as Temporally Disjoint Networks(TDN's).

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v. Octagon :

Developed by STMicroelectronics in a Direct Network with an Octagonal topology[14]. It consists of 8 nodes and 12 bidirectional links and was designed to meet the requirements of network processor SoCs , such as Internet Router Implementation. The Octagon can operate either Packet (or) Circuit Switched mode. In Packet Switched mode, the nodes route according to a destination field in each Packet. In Circuit Switched mode, can operate network arbiter allocates the path between the 2 nodes that must communicate with each other. The Octagon architecture has been generalized to a polygon with diameters and this extension has been named as Spidergon.

vi. QNoC :

The Quality of Service NoC(QNoC)[15] developed by Technion in Israel, is a Direct Network with an Irregular Mesh Topology. It uses WH Switching with a Link-to-Link credit based Flow control scheme, and XY- minimal routing scheme. A Packet in QNoC consists of 3 parts : Target routing address, a command, payload. The traffic is divided into 4 different classes (or levels) :Signaling, Real- time, Read/Write, Block-Transfer, with signaling having the highest priority and block transfers the lowest priority. Instead of providing a Hard Guarantee on Service, QNoC provides a Statistical Guarantee.

vii. SOCBUS :

The SOCBUS[16] NoC, Developed at Linkoping University, is a Circuit Switched Direct Network with a 2D Mesh Topology. A Minimum Path LengthRouting Algorithm is used.

viii. SPIN :

The Scalable Programmable Integrated Network (SPIN)[17] is a Packet Switched indirect network thatimplements a Fat-Tree Toplogy, with two one-way 32-bit Link Datapath. It makes use of WH Switching, deflection routing, and packet reordering at the receiver NI. Thus, GS(Guaranteed Service) are not Supported , and only BE(Best Effort)QoS IS Offered in SPIN.

ix. Xpipes :

Xpipes along with the accompanying Net chip complier(a combination of Xpipes Complier) weredeveloped by the University of Bologna and Standford University. Xpipes[18] uses Source based Routing, WH Switching and supports the OCP standard for interfacing nodes with the NoC fabric.Xpipes also supports design of Heterogeneous, Customized network topologies. The Xpipes Compiler is a tool that automatically instantiates an NoC communication infrastructure using Xpipe components.

NoC Architecture	AEthereal (developed by Philips) [3-7]	HERMES (developed by Faculdade de informatica PUCRS,Brazil) [9,10]
Network Topology	Synchronos Indirect network(butalso supports irregular)	Direct Network with 2-D Mesh Topology
Switching Startegies	WH Switching	WH Switching
Routing Algorithm	Contention Free Source Routing based TDM	Minimal XY Routing Algorithm
Flow Control Scheme	Credit-based flow control scheme	---
Clocking Scheme	Synchronous	---
Quality of Service	GT(Guaranteed Throughput)as wellas BE(Best Effort) QoS.	---

Table – 2 : Comparison of NoC Architectures AEthereal, HERMES

NoC Architecture	MANGO (developed by Technical University of Denmark)	NOSTRUM (developed by KTH in Stockholm)
Network Topology	---	Direct Network with 2-D Mesh Topology
Switching Startegies	Circuit Switching	SAF(Store and Forward)Switching implemented by VC Switching

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Routing Algorithm	Guaranteed Routing Services	Hot Potato or Deflective Routing Algorithm
Flow Control Scheme	Flow control with Resource reservation	---
Clocking Scheme	Clockless(Virtual channels to establish virtual end-to-end connections)	---
Quality of Service	BE(Best Effort) aswell as GS(Guaranteed Service)	Hard GS(Guaranteed Service)

Table–3 : Comparison of NoC Architectures MANGO, NOSTRUM

NoC Architecture	Octagon (developed by STMicroelectronics) [14]	QNoC (developed at Technion in Israel) [15]
Network Topology	Direct Network with an Octagonal Topology	Direct Network with Irregular Mesh Topology
Switching Startegies	Packet or Circuit Switched Mode	WH Switching
Routing Algorithm	---	XY Minimal
Flow Control Scheme	---	Link-to-Link Credit-based
Clocking Scheme	---	---
Quality of Service	---	---

Table-4 : Comparison of NoC Architectures Octagonal, QNoC.

NoC Architecture	SOCBUS(developed by Linkoping university)	SPIN	Xpipes(developed by the university of Bologna and Standford)
Network Topology	Direct Network with 2-D Mesh Topology	Indirect Network	Irregular Topology
Switching Startegies	Circuit Switched Mode	Packet Switching	WH Switching
Routing Algorithm	XY Adaptive	Static and Dynamic Routing Algorithm	Source-based Routing
Flow Control Scheme	---	Link-Level Flow Control Scheme	---
Clocking Scheme	---	---	---
Quality of Service	---	BE(Best Effort)	---

Table-4 : Comparison of NoC Architectures Octagonal, QNoC.

The NoC Architecture Comparison are tabulated above in Table -2, Table – 3, Table – 4.The Net chip Complier, which builds upon the Xpipes Complier, has been validated for different topologies such as Mesh, Torus, Hypercube, Clos, and Butterfly.

The NoC architectures offer varying Levels of QoS, and are Scalable to meet the needs of emerging high performance multiprocessor systems. The design Structure, Regularity and Predictability offered by NoC architecture allows designers to take a system level view of On-Chip Communication and make design choices that can withstand the variability that plagues DSM technologies. Some Semiconductor design houses such as STMicroelectronics and Philips have been experimenting with using NoC's intheir Designs.

The Power consumption is several times greater than for current bus – based approaches, due to the need for several complex NI and Switching / Routing Logic Blocks. The choice certain protocols to ensure reliable data transmission can also lead to

excessive power dissipation circuit and architecture innovationsare needed to reduce this power gap.

The Latency in NoC's offers a Superior bandwidth compared to bus-based schemes, the latency response still lags behind that can be achieved with bus-based and dedicated wiring approaches. An increase in latency occurs decrease of the additional delay to packetize/de packetize data at the NI'sa Innovative Flow control strategies, lower diameter topologies, and native NoC support are needed to ensure that hard latency constraints are satisfied. Even circuitswitching is used, there are overheads involved.

The NoC design space is enormous, with numerous topologies and protocol/ parameter choices for switching strategies, Flow control, etc. The design space exploration and implementation tools and flows are needed that can be integrated with standard tool flows used today to enable the usage of NoC technology. There is also a need for s open benchmarks to compare the performance, cost, reliability and other features of different NoC architectures, to select the one most suited for an application.

Exploration and Verification typically require simulation of design in order to better understand, Optimize and verify the behavior of an application at execution time. Due to large size of systems that will require NoC's, and the GHz Frequency ranges are possible on Network – on – Chip Links. Innovative Strategies are needed that improves the simulation Speed. The technique such as distributed simulation over multiple workstations and partial FPGA- prototyping.

V. CONCLUSION

The On-Chip Communication Architecture improves the Scalability and Performance of overall System. The Evolution of On-Chip Communication architectures are improved by the usage of hundreds to millions of components on the chip. Thus, the Network-on-Chip(NoC)consists of processing element(PE), Network Interface(NI) and Router. The Design Problems of NoC are Tradeoff between Performance, Power, Cost, Area, and Reliability. Thedesign open problems are Latency, Power , lack of tools and Simulation Speed.

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