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# Comparative Performance Analysis of Logic Gates Using CMOS and FinFET Technology

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***Abstract: Logic gates such as AND, OR, NOT, XOR and NAND are basic building component in designing logical circuits. The performance of these gates decides the performance of the designed circuits. The compact design, ability to work at higher frequencies or speed and power efficiency are major parameters that decide the viability of any logic gate. In this paper, a comprehensive comparative performance analysis of the basic gates based on conventional CMOS and FinFET technologies have been carried out and compared. The simulation results show that FinFET technology give better performance in terms of design area, delays and power consumption. So, the performance of digital computers and logic circuits can be enhanced by using FinFET based gates.***
***Keywords: OR, AND, NOT, XOR, NAND, NOR, FinFET, CMOS.***

## I. INTRODUCTION

VLSI (Very Large Scale Integrated) circuits are required for the development of high-performance, portable electronics. VLSI technology relies heavily on performance parameters such as speed, area, cost, and power. The fundamental logic gates serve as the foundational elements and building blocks for VLSI digital logic circuits based on combinational logic. Logic gates are used to perform binary computations in the adder and multiplier blocks, as well as comparators, compressors, code converters, error detectors or correctors, and parity checks [1].

The circuit runs on two voltage levels that are split into logic levels known as logic 0 and logic 1. Depending on the logic of the gate, applied inputs of logic 0 or logic 1 will result in gate replication. AND, OR, and XOR are the basic logic gates covered in this paper. The gates can be built in a variety of ways, with Complementary Metal Oxide Semiconductor (CMOS) being one option. As performance measurements, the gates with these design types are compared in terms of power, delay, speed, and area. The name "logic" itself suggests that they engage in specific logical operations. Logic gates can be combined to create physical representations of any imaginable calculation or algorithm using electrical, optical, mechanical, or even biological devices. In general, each logic gate has a single output, nevertheless the number of inputs can vary. However, the logic gate known as "NOT" only has one input and one output. Diodes and transistors are employed as the building blocks of logic gates, which are used in digital circuits. Highly complex operations can be carried out by fusing thousands or millions of logic gates. We can better illustrate how a logic gate works by using a truth table. For every conceivable combination of input states, it displays the output states [2].

## II. DESIGN TECHNOLOGY

The CMOS technology (MOSFET) is by far the most popular transistor in both digital and analogue circuits because it is a very mature technology and has the ability to switch on with a very low threshold current (less than 1 mA) while providing a much higher threshold current to a load (10 to 50A or more). However, a higher gate voltage (3–4V) is needed for the MOSFET to turn on. Thus, has speed and power efficiency both which is excellent for switching applications [3].

The use of FinFET technology in integrated circuits has recently expanded dramatically. FinFET transistor technology has several

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significant advantages in IC design over more traditional CMOS planar technology. FinFET technology promises to provide the enhanced scalability required to maintain current advancements in integrated circuits with higher degrees of integration. FinFET offer an excellent subthreshold slope and higher voltage gain. In FinFET the channel has been lengthened, very little current can escape through the body of the device when it is in the "off" state [4]. Additionally, it permits the use of lower threshold voltages, which enhances performance and reduces power dissipation. Fast switching times in FinFETs can be attributed to a larger drive current. The length of the gate has an important role in decreasing leakage current and thereby leakage power. FinFETs have sufficient gate length because the gate is wrapped around the drain-source channel, and there is no leakage current when the gate is not active. Nevertheless, leakage current exists in MOSFETs as the gate is scaled down [5].RESULTS AND DISCUSSION

### a. NOT/INVERTER

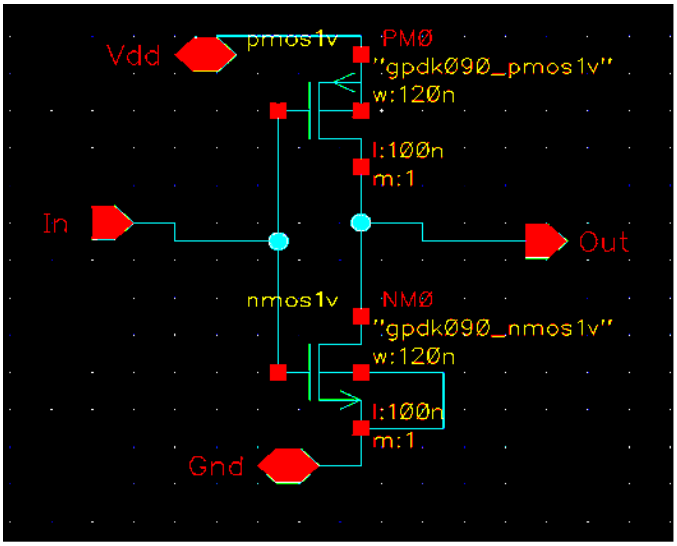


Fig:5
**Schematic of NOT gate**

### b. AND Gate

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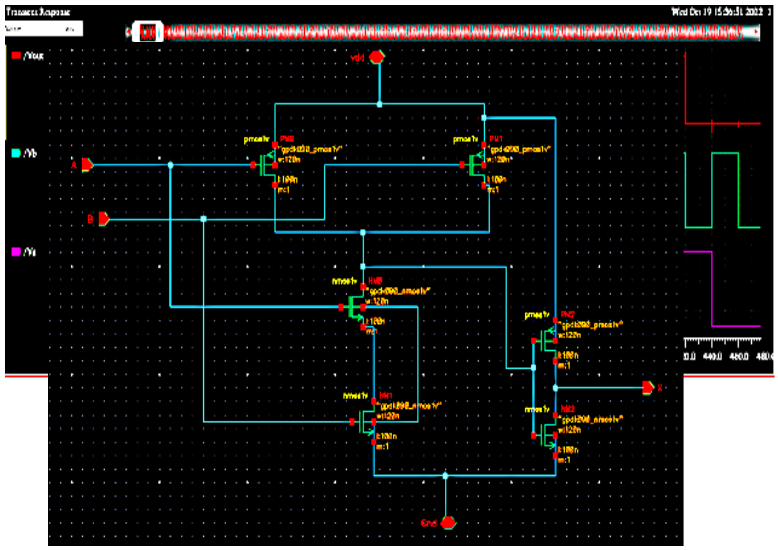

Fig:8
**Schematic of 2-input AND gate**

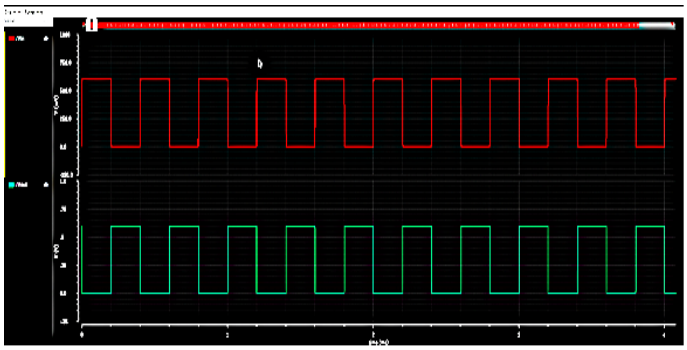

Fig:6

**Simulation For CMOS**

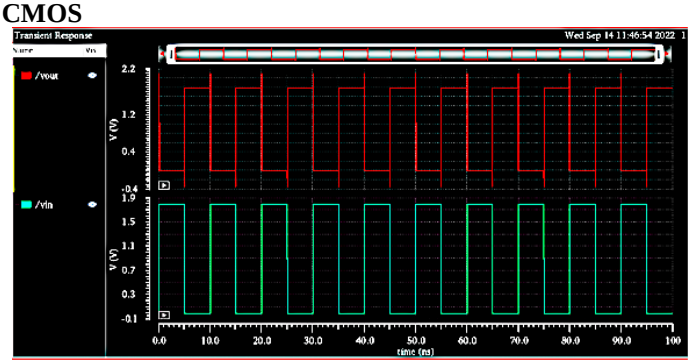


Fig:7
**Simulation For FinET**

Fig:9

**Simulation For CMOS**

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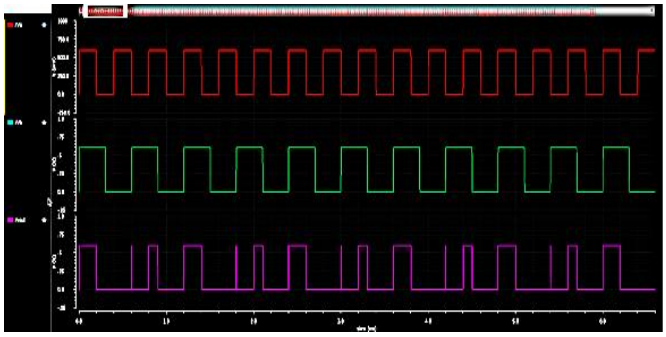

Fig:10
**Simulation For FinFET**

### c. OR Gate

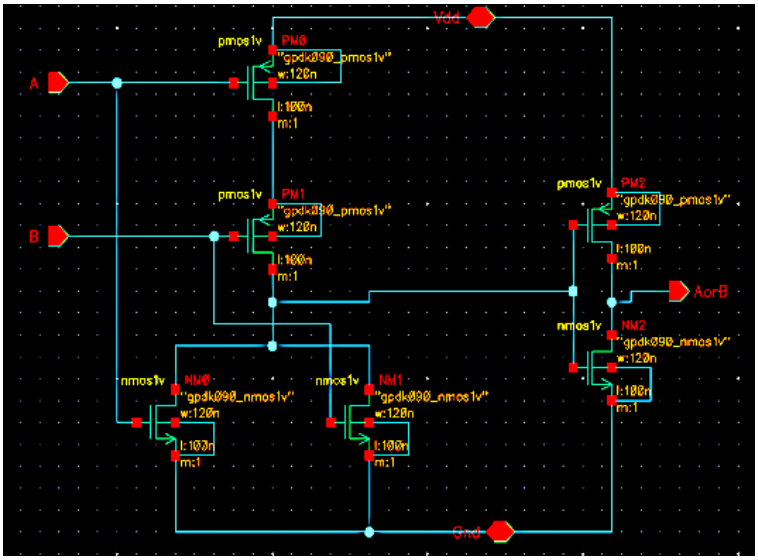


Fig:11
**Schematic of 2-input OR gate**

### d. XOR Gate

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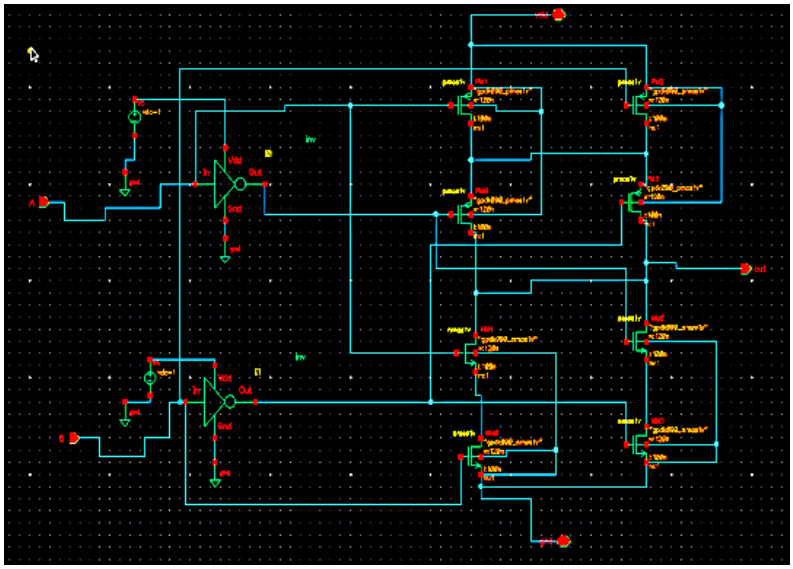
Fig:14



**Schematic of 2-input XOR gate**

## III. COMPARITIVE ANALYSIS

Both the CMOS and FinFET technologies are used in the design of the logic gates in this paper. The simulation study has been performed using Cadence Virtuoso tool. For the two technologies for various basic gates, the parameters—such as minimum design space, delay, and power consumption—are measured, analysed and compared. The measured results are represented in tabulations 7 and 8, for CMOS and FinFET technologies, respectively. The graphical representations of various parameters are also shown in figures from Fig. 17–22. The parameters such as average power, delay and power-delay- product (PDP) are measured at two voltages 0.6V and 0.9V for both the technologies. From the tables it is obvious that XOR

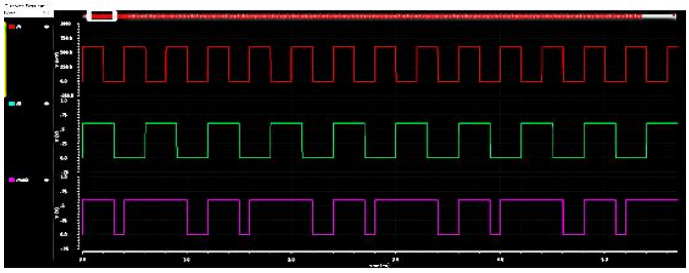


Fig:12

**Simulation For CMOS**

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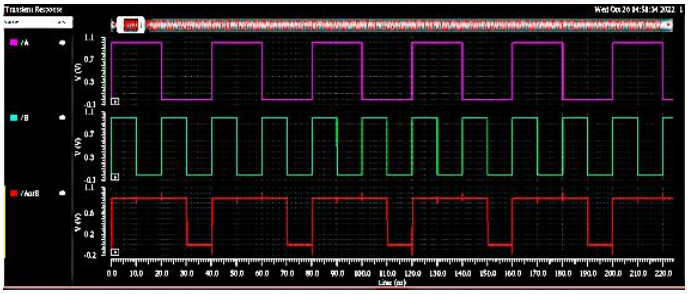

Fig:13
**Simulation For FinFET**

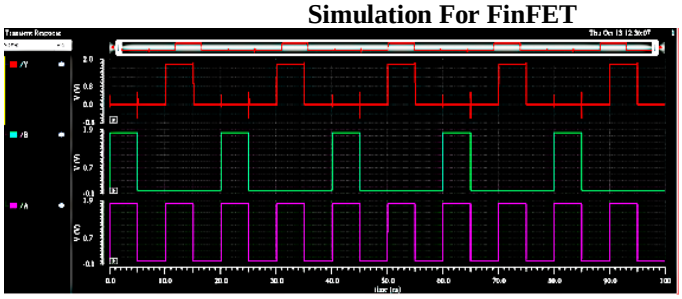

Fig:15
**Simulation For CMOS**

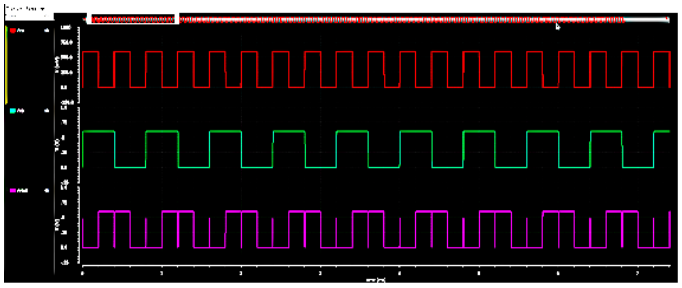

Fig:16
**Simulation For FinFET**

consumes the maximum power and is slowest among all gates, while INVERTER is least power consuming and fastest. Interestingly, the OR gate is superior than AND gate in the measured parameters. When the supply is increased delays are decreased because the charging and discharging of internal capacitors are faster due to increased current. But this increased current increases the power consumption also. PDP also increases because the increment in power consumption more than the decrement in delay, therefore the net PDP increases with the supply voltage. The performance of gates is drastically enhanced when FinFET technology is used in their design. The superior multi-gate control, lesser internal

resistance and capacitances as well as lesser parasitic elements of FinFET technology are responsible for the performance enhancement. The power consumption, delay and PDP are many orders lesser for FinFET technology compared conventional CMOS technology. For example, these parameters are 96.4e-6, 38.7e-9, 373e-14 and 99.5e-9, 18.1e-12, 180e-20 for CMOS and FinFET technology for inverter gate at 0.6 V, respectively. Similarly, for other gatesthe FinFET technology is much superior to conventional CMOS technology. The performance is even better at higher supply voltages. The corresponding comparison of the parameters such as power consumption, delay and power- delay-product (PDP) are also plotted and shown in figures from Fig.15-22. From the output graphs, it can be clearly seen that FinFET technology performances are excellent and superior to conventional CMOS technology.

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| **CMOS Technology** | $V_{DD}$ = 0.8V | | | $V_{DD}$ = 1.2V | | |
|---|---|---|---|---|---|---|
| | PDP | Time delay | Average Power | PDP | Time delay | Average Power |
| INVERTER | 373.06e-14 | 38.7e-9 | 96.4e-6 | 486.1e-14 | 19.5e-9 | 249.3e-6 |
| AND | 815.18e-14 | 52.9e-9 | 154.1e-6 | 851.8e-14 | 28.3e-9 | 303.2e-6 |
| OR | 736.4e-14 | 48.1e-9 | 153.1e-6 | 1464.02e-14 | 38.7e-9 | 378.3e-6 |
| XOR | 2020.8e-14 | 68.48e-9 | 295.1e-6 | 2294.39e-14 | 51.1e-9 | 449e-6 |

Table 7: Comparative analysis of logic gates with reference to power & delay using CMOS Technology

| **FinFET Technology** | $V_{DD}$ = 0.8V | | | $V_{DD}$ = 1.2V | | |
|---|---|---|---|---|---|---|
| | PDP | Time delay | Average Power | PDP | Time delay | Average Power |
| INVERTER | 180.09e-20 | 18.10e-12 | 99.5e-9 | 142.40e-20 | 9.5e-12 | 149.9e-9 |
| AND | 546.95e-20 | 36.12e-12 | 151.3e-9 | 577.76e-20 | 25.69e-12 | 224.9e-9 |
| OR | 596.63e-20 | 38.97e-12 | 153.1e-9 | 440.18e-20 | 15.73e-12 | 279.84e-9 |
| XOR | 31.39e-22 | 104.5e-15 | 299.9e-9 | 496.60e-22 | 110.7e-15 | 448.6e-9 |

Table 8: Comparative analysis of logic gates with reference to power & delay using FinFET Technology

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## a. GRAPHICAL ANALYSIS, AVERAGE POWER

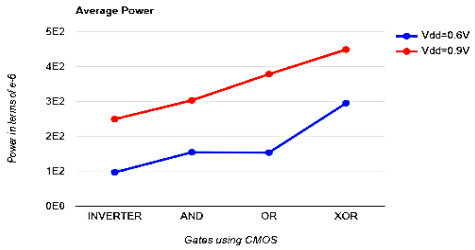



Fig:17
**CMOS**

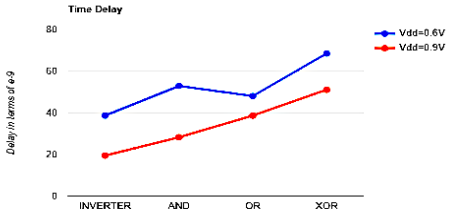



Fig:18
**FinFET**

## b. POWER DELAY PRODUCT (PDP)

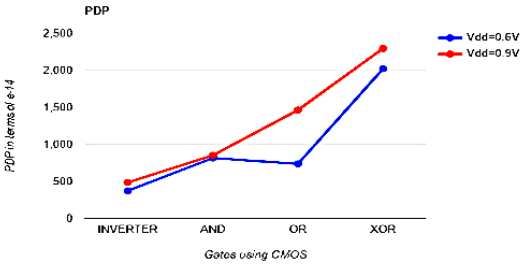



Fig:19
**CMOS Technology**

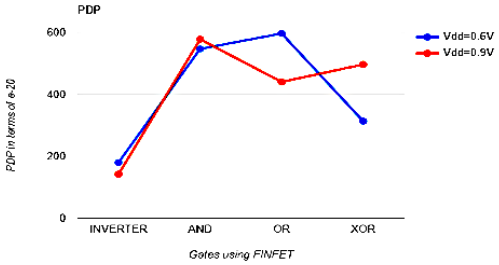
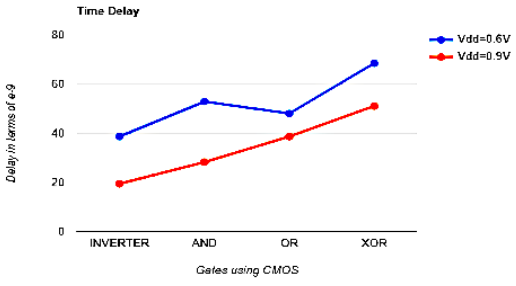



Fig:20
**FinFET Technology**




## c. DELAY

Fig:21
**CMOS Technology**

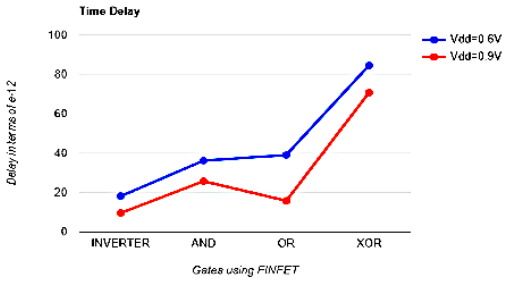



Fig:22
**FinFET Technology**

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## IV. CONCLUSION

The simulation analysis of basic logic gates such as AND, OR, XOR, and NOT has been done using the CMOS and FinFET technology under similar conditions of supply and input voltages. The circuit parameters such as power consumption, delay and power-delay-product for the mentioned gates are measured at different supply voltages and analyzed. It is observed that FinFET technology is far superior compared to conventional CMOS one in terms of design space, delay and power consumptions. So, performance of logic circuit made of these gates will be enhanced by FinFET technology.

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