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CMOS and FinFET-based Multiple Bit Full Adder Circuits: Comparison and Analysis

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Abstract*—The FinFET based devices and components could be crucial for Moor law as it endorse the characteristic requirements of less design space low power consumption and high performance. All these characteristics make this technology desirable for IC technology compared to conventional CMOS technology. In this paper a comprehensive simulation study has been carried out for full adder using conventional CMOS and FinFET technology. The obtained results show that FinFET performance are better compared to CMOS by many orders.

***Keywords*—**MOSFET, FinFET, Cadence, Adder.

I. INTRODUCTION

Transferable devices with high speed, small size, great reliability, low power consumption, and longer battery life have increased the use of VLSI [1]. The main issue with complex devices is the transistor count because it directly affects the device's area and speed. Arithmetic operationsare frequently used in many VLSI applications, including digital signal processing, image and video processing, and microprocessors. Therefore, the use of the arithmetic modules has a significant impact on the performance of integrated circuits.

A complete adder is the most important component of complex arithmetic circuits since adding two binary integers is the primary action in an arithmetic logic unit. The constant scaling of transistor size and lowering of operating voltage is what has allowed integrated circuits to significantly improve their performance. Because of the technology's quick scaling to the deep sub-micron level, the circuit's speed increases significantly. The power consumption per chip likewise increases significantly as chip density increases. Therefore, low-power and high-speed are the two key characteristics that must be taken into account while designing current VLSI circuits require quick calculation using the least amount of power, hence VLSI circuits with the ideal level of delay and power [2].

Full adders have become a hot topic in the field of VLSI circuit design due to its significance in the Arithmetic Logic Unit (ALU) of digital signal processing chips and the micro- processors. As a result, various adder cell types have been created over time, each with unique benefits and drawbacks. Complementary pass logic (CPL), which uses only n-channel CMOS (nMOS) to build entire adder cells, was used in the early stages of VLSI architecture. However, static complementaryCMOS (C-CMOS), which used both p- channel CMOS (pMOS) and (nMOS) transistors, supplanted CPL due to excessive power loss and transistor count. As a result, various types of adder cells have been created over time, each with unique benefits and drawbacks [3]. Many research has been conducted to develop devices with more sophisticated features in order to improve the performance of full adders in terms of these qualities. For applications requiring high speed and low power, conventional MOSFETs have been enhanced. Numerous studies have also produced additional beneficial technologies, such as the Fin-type Field Effect Transistor (FinFET) [4].

The CMOS technology (MOSFET) is by far the most popular transistor in both digital and analogue circuits because it is a very mature technology and has the ability to switch on with a very low threshold current (less than 1 mA) while providing a much

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higher threshold current to a load (10 to 50A or more) [5][6]. However, a higher gate voltage (3–4V) is needed for the MOSFET to turn on. Thus, has speed and power efficiency both which is excellent for switching applications. The use of FinFET technology in integrated circuits has recently expanded dramatically. FinFET transistor technology has several significant advantages in IC design over more traditional CMOS planar technology [7].

FinFET technology promises to provide the enhanced scalability required to maintain current advancements in integrated circuits with higher degrees of integration. FinFETs provide a superior subthreshold slope and higher voltage gain. In FinFET the channel has been lengthened, very little current can escape through the body of the device when it is in the "off" state [8]. Additionally, it permits the use of lower threshold voltages, which enhances performance and reduces power dissipation. Fast switching times in FinFETs can be attributed to a larger drive current. The length of the gate has an important role in decreasing leakage current and thereby leakage power. FinFETs have sufficient gate length because the gate is wrapped around the drain-source channel, and there is no leakage current when the gate is not energized. Nevertheless, leakage current exists in MOSFETs as the gate is scaled down [9].

II. SIMULATION RESULTS

Full adder is a type of adder that adds three inputs and gives two outputs. Out of three, two will be the present inputs and the third input will be the carry from the previous stage. Full adder is shown in Fig 1, where ‘A’ and ‘B’ are the actual inputs, and 'C' is the carry from the previous operation. SUM and CARRY OUT are the two outputs. The Truth Table shown in Table 1 gives an idea of outputs for various input combinations. To study the performance of multi-bit adders, 2-bit and four-bit adders are also investigated. The 2-bit adder has been obtained cascading two 1-bit adders and a 4-bit adder is obtained by cascading two 2-bit adders, and the schematic are shown in Fig.1, Fig.2 and Fig.3, respectively.

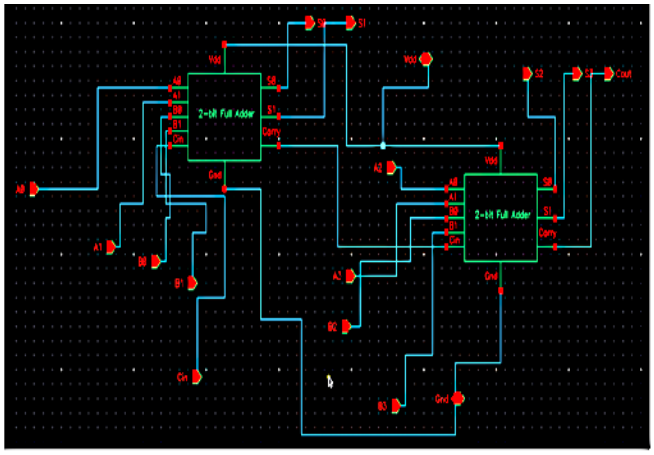

Fig:1 1-Bit Full adder using basic gates

We done multi bit full adders and compared them with CMOS and FinFET technology, because a computer is a calculating device in and of itself, the full adder is crucial to the calculation. As a result, it uses both complex circuitry and such circuits.

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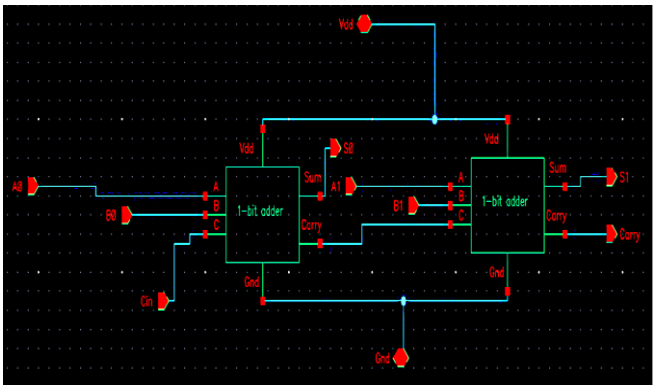

Fig:2 2-Bit adder cascading two 1-bit adders

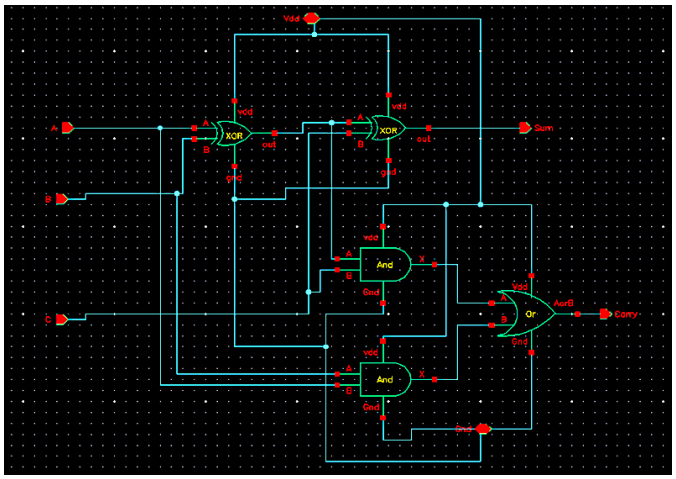

Fig:3 4-Bit adder cascading two 2-bit adders

a. 1-BIT FULL ADDER

The symbol of the conventional 1-bit full adder is shown in Fig:4. The proposed adder simulation results are shown in Fig:5 and Fig:6.

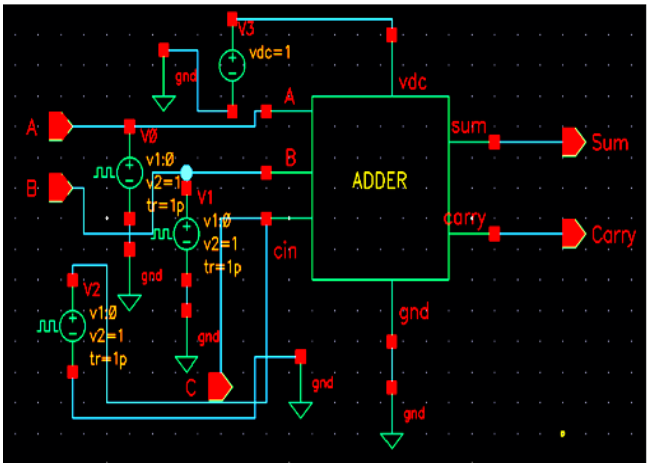

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Fig:4 Symbol of a 1-bit full adder

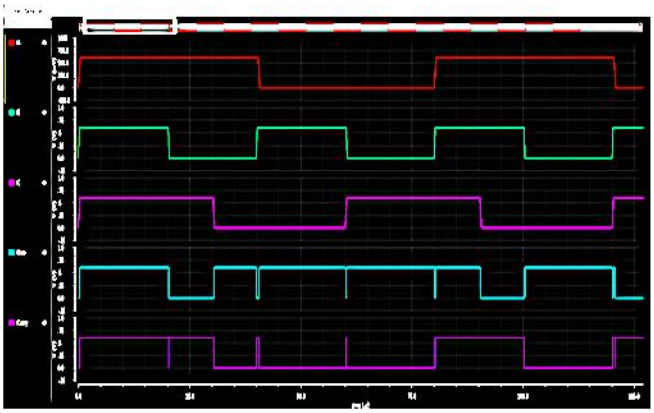

Fig:5 Output for Full adder (using FinFET technology)

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Fig:6 Output for Full adder (using CMOS technology)

b. 2-BIT FULL ADDER

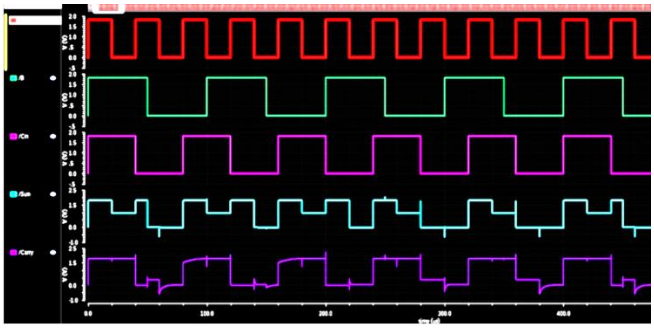

Figure:7 shows the symbol of the conventional 2-bit full adder. The proposed adder simulation results are shown in Fig:8 and Fig:9

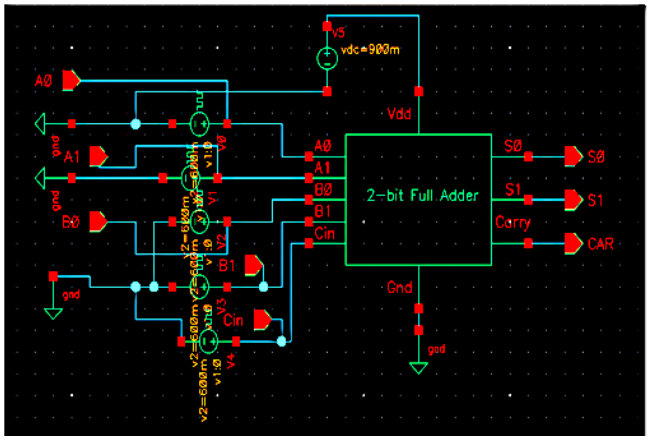

Fig:7 Symbol of a 2-Bit Full Adder using

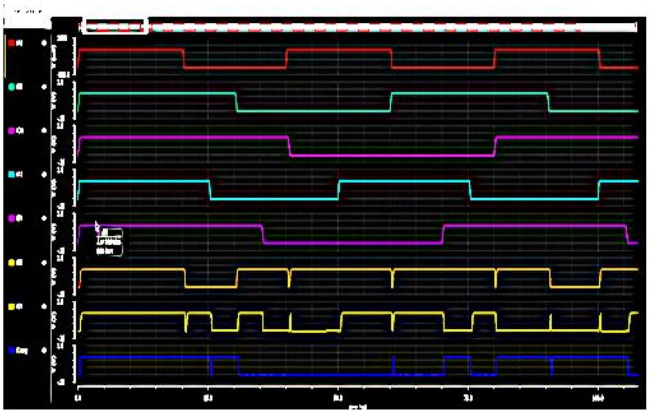

Fig:8 Output for 2-Bit Full Adder (using FinFET technology)

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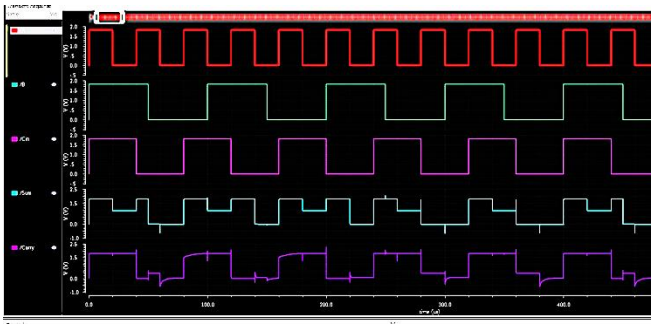

Fig:9 Output for 2-Bit Full Adder (using CMOS technology)

c. 4-BIT FULL ADDER

Figure:10 shows the symbol of the conventional 4-bit full adder. The proposed adder outputs are shown in Fig:11 and Fig:12.

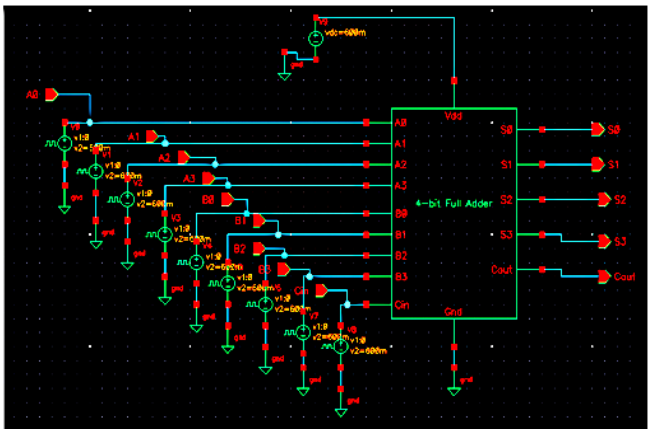

Fig:10 Symbol of 4-Bit Full Adder

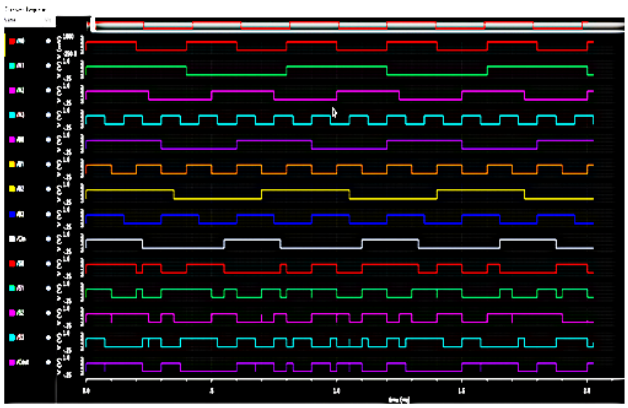

Fig:11 Output for 4-Bit Full Adder (using FinFET technology)

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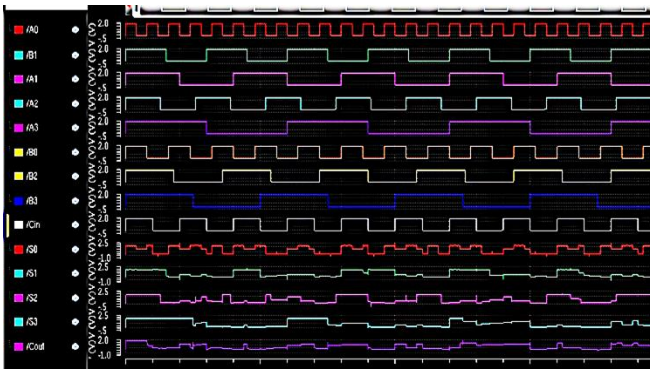

Fig:12 Output for 4-Bit Full Adder (using CMOS technology)

III. COMPARITIVE ANALYSIS

CMOS Technology	V_{DD}=0.8V			V_{DD} =1.2V		
	PDP	Time delay	Average Power	PDP	Time delay	Average Power
ONE BIT FULL ADDER	2530.08e-14	79.09e-9	319.90e-6	3161.28e-14	59.3e-9	533.1e-6
TWO BIT FULL ADDER	6.2e-12	19.79e-6	313.3e-6	7518.9e-12	12.43e-6	604.9e-6
FOUR BIT FULL ADDER	13.52e-12	24.79e-6	545.5e-6	13777.58e-12	15.47e-6	890.6e-6

Table:1 PDP, Time delay and Average power comparison of 1-Bit,2-Bit,4-Bit Full Adders

FinFET Technology	V_{DD} =0.8V			V_{DD} =1.2V		
	PDP	Time delay	Average Power	PDP	Time delay	Average Power
ONE BIT FULL ADDER	180e-16	40e-9	451.9e-6	8741.47e-20	118.4e-12	738.3e-9
TWO BIT FULL ADDER	404.54e-14	101.9e-9	39.7e-6	6611.6e-14	100.1e-9	660.5e-6
FOUR BIT FULL ADDER	960.48e-14	200.1e-9	48e-6	6802.53e-14	101e-9	673.5e-6

Table:2 PDP, Time delay and Average power comparison1-Bit,2-Bit,4-Bit Full Adders

Based on the Table:1 provided, we compared the performance of 1-bit, 2-bit, and 4-bit full adders using CMOS technology at two different supply voltages (0.8V and 1.2V). The key metrics of comparison are the power delay product (PDP), time delay, and average power consumption. It can be observed that the average power, delay and power-delay- product (PDP) are increasing from 1-bit to 4-bit adders which is obvious because number of stages and therefore, the number of gates is increasing. When comparing the results at 0.8V and 1.2V, we can see that the PDP and time delay generally decrease as the supply voltage increases.
This trend is expected since higher voltage levels provide more current which decreases the charging and discharging of the internal capacitance and therefore faster switching times. However, the average power consumption increases with the supply voltage.

Overall, the choice of full adder design depends on the specific application requirements and trade-offs between performance and power consumption. In general, larger full adders will provide better performance but at the cost of higher power consumptionFrom Table:2 Full adders using FinFET technology at a supply voltage of 0.8V. The key metrics of comparison are the power delay product (PDP), time delay, and average power consumption.
From the table, we can see that the PDP and time delay are generally lower for FinFET-based full adders compared to CMOS-based full adders at the same voltage level. This is expected since FinFETs have a better electrostatic control and shorter channel length, resulting in faster switching times and lower power consumption. However, the average power consumption is higher for FinFET-based full adders, which is a trade-off for the improved performance.
When comparing the results for different sizes of full adders, we can see that the PDP and time delay generally increase as the size of the full adder increases. However, the average power consumption remains relatively constant across different sizes of full adders.
Full adders using Fin`FET technology at a supply voltage of 1.2V. Comparing the results with the 0.8V case as shown in Table:3, we can see that the PDP and time delay generally increase as the voltage level increases. This is expected since higher voltages result in higher power consumption and longer switching times. However, the average power consumption decreases for the 1-bit full adder, while it increases for the 2-bit and 4-bit full adders. This is because the average power consumption is affected by both the PDP and the time delay, and the trade-off between these factors changes with the voltage level. When comparing the results for different sizes of full adders, we can see that the PDP and time delay generally increase as the size of the full adder increases. However, the average power consumption varies across different sizes of full adders.
Overall, the choice of full adder design depends on the specific application requirements and trade-offs between performance and power consumption. FINFET-based full adders can offer improved performance compared to CMOS- based full adders but at the cost of higher power consumption. It is important to consider the specific needs of the application to determine the optimal design choice.

IV. CONCLUSION

In conclusion, the comparison and analysis of CMOS and FINFET-based full adder circuits were performed in terms of average power consumption, time delay, and power delay product at 0.8V and 1.2V supply voltages. The simulations are carried out using Cadence software at room temperature. The results showed that FINFET-based full adders outperformed CMOS-based full adders. However, FINFET- based full adders require more complex fabrication processes and higher costs compared to CMOS-based full adders. Therefore, the choice between CMOS and FINFET-based full adders depends on the specific design requirements and cost considerations. For a mature fabrication technology FINFET technology is superior to existing MOS technology.

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