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DESIGN AND IMPLEMENTATION OF 3T BASED XOR/XNOR LOGIC GATE FOR HIGH POWER GAIN AND LESS PROPAGATION DELAY

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Abstract

In this paper, a 4:1 multiplexer with a 3T-based xor\xnor logic gate is proposed using 25-nanometer technology having high power gain and less propagation delay. The proposed circuits are highly optimized in terms of power consumption and time delay due to low output capacitance and low short-circuit power dissipation. The Micro Wind EDA simulation tool is used to design the cascade logic xor\xnor circuit. The proposed circuits are investigated for different parameters such as the supply voltage, threshold voltage, output capacitance, internal noise, and propagation delay.

Keywords

Arithmetic Logic Unit(ALU), Multiplier(MUX), Electronic Design Automation(EDA),3T (Transistor)

Introduction

Logic gates are used in microcontrollers, microprocessors, electronic and electrical project circuits, and embedded system applications. The basic logic gates are categorized into seven types AND, OR, NAND, XOR, XNOR, and NOT. These are important digital devices, mainly based on the Boolean function. Low-power applications have emerged as an arena of prime concern for VLSI designs. Together with that, the high-speed full adder that uses low power consumption has indisputably one of the most crucial components of a processor because they are mostly used in arithmetic logic units (ALU).

The semiconductor industry has witnessed explosive growth in sophisticated multimedia-based applications integrated with electronic gadgetry since the last decade. Fast arithmetic computation cells including address multiplexers are the most frequently and widely used circuits in very large-scale integration systems. The XOR/XNOR circuits are basic building blocks in various circuits expertly arithmetic circuits, multipliers, comparators, priority checkers, code converters, error detecting or code detecting codes, and face detector. So the efficiency of Xor/Xor and Xor/Xnor multiplier is more important for the implementation of a new multiplier using an advanced 3 input xor gate. This 3 input xor is used to design the complex Xor mux and Xnor mux by using Microwind 3.9 EDA tool. This tool is used to design the structure of the logic gates, also it is used to reduce power consumption compared to complex CMOS mux.

XOR gate: The XOR gate gives an output of 1 if either both inputs are different, it gives 0 if they are the same. For the n-input gate if the number of input 1 is odd then it gives 1 otherwise zero.

XNOR gate: The XNOR gate gives an output of 1 if both inputs are the same and 0 if they are different. For the n-input gate, if the number of input 1 is even then it gives 1 otherwise zero.

The XOR/ XNOR and XOR – XNOR circuits evaluation revealed that using the NOT gates on the critical path of a circuit is a disbenefit. Another disadvantage of a circuit is to have positive feedback on the labors of the XOR – XNOR gate for compensating the affair voltage position. This feedback increases the detention, affair capacitance, and, as a result, the energy consumption of the circuit also.

LITERATUR SURVEY

Hamednaseri and Somayeh Timarchi et al discussed Low Power and Fast Full Adder by Exploring New Xor and Xnor Gates new XOR/ XNOR and XOR – XNOR gates that don't have the mentioned disadvantages. eventually, by using the proposed XOR and XOR – XNOR gates, we offered six new FA cells for colorful operations. Also, a modified

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system for transistor sizing in digital circuits was proposed. The new system utilizes the numerical calculation PSO algorithm to opt the applicable size for transistors on a circuit and also it has truly good speed, delicacy, and confluence. After pretending the FA cells in different conditions, the results demonstrated that the proposed circuits have a truly good performance in all simulated conditions.(1)

Yadhav, Deepa(AP), et al discussed performance analysis of xor and xnor gates using different sense styles, adder circuit is introductory part of computation circuits and also operation Specific Integrated Circuits(ASIC). Combination of unique sense styles are used to apply adder circuits. Performance of these circuits is depend on XOR and XNOR circuits. In this unit, XOR and XNOR enforced using PTL, CPL cross coupled and PTL cross coupled sense styles.(2)

Anum Khan and Subodh Wairya et al discussed Performance Evaluation of largely Effective Xor and Xor-Xnor Topologies using CNTFET for Nano calculation With inordinate scaling in the VLSI assiduity, the Carbon Nanotube Field Effect Transistor(CNTFET) is arising as a implicit relief to traditional MOSFET technology. XOR gate is an essential element in colorful digital sense circuit designs. thus it's pivotal to concoct a high performing XOR gate and XOR- XNOR gate to increase the overall effectiveness of colorful XOR grounded digital circuits. This paper investigates the performance of several designs of individual XOR gates as well as contemporaneous XOR-XNOR circuits for different operations. The enforced circuits have been anatomized and compared by parameters videlicet transistor count, detention, power dispersion, and power- detention product, and Energy detention product.(3)

Aishwarya.H,Akhila.M,B.G.Manasa et al discussed High-Speed mongrel- sense Full Adder using High Performance 10- T Xor – Xnor Cell The main end of our work is to achieve low power, high speed design pretensions. The proposed mongrel adder is designed to meet the conditions of high affair swing and minimal power. Performance of mongrel FA in terms of detention, power, and driving capability is largely dependent on the performance of XOR-XNOR circuit. In cold-blooded FAs maximum power is consumed by XOR- XNOR circuit. In this paper 10T XOR-XNOR is proposed, which give good driving capabilities and full swing affair contemporaneously without using any external inverter.(4)

Ambati Suneel Kumar, Dayasagar Chowdary et al discussed Low Power Full Swing Xor and Xnor Structures For Full Adder Circuits, As the scale of integration increases, the usability of circuits is confined by the further quantities of power and area consumption. The growing fashionability demands for battery operated bias similar as mobile phones, tablets and laptops. By reducing the number of transistors in the conventional circuits we've proposed two full adder circuits which is having advantage of consuming low power when compared to the other two conventional circuits. In this design XOR- XNOR gates are used to apply full adder structures. These circuits are going to be optimized in terms of power consumption and detention, which are due to low affair capacitance adder. One- bit full adder circuit is proposed grounded on new full- swing XOR- XNOR gates.(5)

Dharani D, NareshKumar.K,Vineela.M et al discussed Design of Xor/ Xnor Circuits for mongrel Full Adder Increased operation of battery- operated compact bias similar as scrapbooks, Smart phones,e-readers, MP3 players and numerous other bias are designed with erected- in storehouse, lower silicon area, longer battery life, advanced speed and further trustability. Full adder is being dominant block in computation operations. The main block of the full adder circuit is the XOR/ XNOR gate, as the XOR/ XNOR gate consumes further power. The power consumed by the full adder is thus reduced by optimizing the design of the XOR/ XNOR gates. These can be used in a variety of multipliers, similar as Vedic, Wallace, Array.(6)

M.Kamaraju,K.Babulu, et al discussed Low- Power and Fast Adders Using New Xor and Xnor Gates,new circuits for XOR/ XNOR and contemporaneous XOR – XNOR functions are proposed. The proposed circuits are largely optimized in terms of the power consumption and detention, which are due to low affair capacitance and low shortcircuit power dispersion. We also propose six new mongrel 1- bit full- adder(FA) circuits and Ripple Carry Adder grounded on the new full- swing XOR – XNOR or XOR/ XNOR gates. Each of the proposed circuits has its own graces in terms of speed, power consumption, power detention product(PDP), driving capability, and so on. To probe the performance of the proposed designs, expansive Mentor plates simulations are performed.(7)

Pygastijuveria,K. Ragini, et al discussed Low Power and High Speed Full Adder Using New Xor and Xnor Gates Six mongrel full adder circuits using new XNOR, XOR gates are proposed in this paper. These circuits are designed to have high speed and lower power consumption compared to being circuits. This is possible due to low affair capacitance. Each bone of the proposed full adder circuit has its own advantages of speed and driving capability.(8)

M.Venkayya Naidu,Y.Saravana Kumar, AlajangiRamakrishna, et al discussed A 45nm Cmos Technology Exploring Low Power and Fast 4 Bit Full Adder Using Xor/ Xnor Gates. The planned circuits area unit extremely optimized in terms of the capability consumption and detention, that area unit thanks to low affair capacitance and low short- circuit power dispersion. We also propose six new mongrel Ripple Carry Adders grounded on the six new mongrel 1- bit full- adder(FA) circuits grounded on the new full- swing XOR – XNOR or XOR/ XNOR gates. Each of the planned circuits has its own deserves in terms of speed, power consumption, power detention product(PDP), driving capability, and so on.(9)

Akhila Krishnan,Dr.V.Balamurugan, Anjana Krishnakumar,Aparna.A,Ashna.A,Athira.M, et al discussed design of Low Power High Speed Full Adder Circuits Using XorXnor Topology, The explosive growth of battery operated movable operations similar as cellular phones,

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smart cards, PDAs, laptops and the elaboration of the loss of the technology requires lower silicon area, high outturn circuitry and most importantly low power.(10)

Mehedi Hasan, Sharnali Islam, Mainul Hossain, HasanU. Zaman et al discussed a Scalable High- Speed mongrel 1- Bit Full Adder Design Using Xor- Xnor Module, High- speed XOR- XNOR- grounded mongrel full adder(FA) using a combination of three sense ways(transmission gate(TG), conventional CMOS(CCMOS), pass transistor(PT)) is presented in this work. Performance analysis and confirmation of the FA design presented in this work have been realized with reference to 10 state- of- the- art FAs. It has been observed that only four being FAs and the proposed FA could be gauged up to 32- bits without including voltage restoration buffers in the internal stages.(11)

Dr.B.S.Sathishkumar et al discussed A Novel Coplanar Grounded Xor/ Xnor Structure for Design of QCA Circuits, Quantum- fleck Cellular Automata(QCA) is a nano scale computational fabric being explored by the Very Large Scale Integration(VLSI) exploration community due to the difficulties in the underpinning of the CMOS transistors. This work uses QCA bias and uses those bias to make a simple field programmable gate array(FPGA). A design rule for technical armature design is presented using programmable bias and introduced a simulation machine tuned to efficiently pretend QCA circuits designed for this armature.(12)

Mouna Karmani1, ChirazKhedhir, Belgacem Hamdi, Amir-Mohammad Rahmani, Ka Lok Man, and Kaiyu Wan et al discussed Design of a Reliable Xor- Xnor Circuit for computation sense Units, Computer systems used in safety-critical operations like space, avionic and biomedical operations bear high dependable integrated circuits(ICs) to insure the delicacy of data they reuse. As computation sense Units(ALUs) are essential element of computers, designing dependable ALUs is getting an applicable strategy to design fault-tolerant computers. In fact, with the nonstop increase of integration consistence and complications ICs are susceptible to numerous modes of failure. Thereby, Reliable operation of ALUs is critical for high performance safety-critical computers.(13)

Rahul Jadia, Sonali Josh et al discussed Design of Low Power Adder Cell By Xor & Xnor Gate, In under this exploration composition, neoteric circuits for Exclusive OR gate and Exclusive NOR gate are designed. The designed sense is largely meliorated in terms of power consummation and speed, which are due to minimal CL at the affair and low leakage power. We followed six new mongrels, one bit one full- adder design grounded on the new Exclusive OR gate and Exclusive NOR(XOR- XNOR) gates.(14)

InumulaVeerarahavaRao,Aditya.M,V.Kavya,Chowdary, K.Sai Nishitha,V.Naveen Sai et al discussed design of Xor and Xnor Grounded Full Adder Circuits, This paper has a XOR/ XNOR gate circuits produces separate and establishes a contemporaneous XOR- XNOR function. Due to stocky yield capacity and short- circuit energy dispersion, the power application and quiescence of these circuits is adding A new one- bit adder mongrel circuit is chosen erected on the effective gates of xor xnor or xor/ xnor. Each prefer circuit has its own advantages as it's known for its high speed, low current drain, short detention product(PDP), galvanic capability.(15)

Sowmya Bhat, Avinash N J, Sandesh Kumar, Bantakal Udupi et al discussed design and Analysis of 8- T and 5- T Grounded Xor and Xnor Gates using Soft Computing Tools, XOR and XNOR gates are the introductory structure block of computation and sense circuits. In the ultramodern period, VLSI technology demands the circuit design with least area consumption, least power consumption and high speed in operation. There are colorful CMOS sense structures available to design digital VLSI circuits, like, pass transistor sense, transmission gate sense, mock NMOS sense, CMOS sense, dynamic and domino CMOS sense, clocked CMOS sense, CVSL sense.(16)

PROPOSED WORK

The 3 input xor gate is designed by using the AND, OR, and NOT gate where 3 input four AND gate, 3 OR gate, and 3 NOT gates is used in cascade form to get the 3 input and single output XOR gate. The 3-input XOR gate is used to design the 4:1 multiplexer for low power loss and high switching speed. The four (3 input XOR) gate is used with the complex structure of a multiplexer designed with an XOR gate. The four (3 input XOR) gate is used with the complex structure of the multiplexer is designed with an XNOR gate.

The 4:1 XOR/XOR multiplexer is designed by using the logic (3 input and 2 input XOR gate). Also, the schematic diagram is formed by using the logic gate with 4 inputs and dual (S0, S1) with NOT gate structure. The In1, In2, In3, and In4 are pinned with a switch and make a binary sequence. Also, s1 and s0 are used to switch the circuit by using the schematic diagram. The (In1,In2,In3) ,(In4,In5,In6),(In7,In8,In9),(In10,In11,In12) are pinned in AND gate. The output (O1, O2) is pinned with 2 input gates (In13, In14). The output of 3 pins AND gate (O3, O4) is pinned with 2 input OR gates (In15, In16) and the (O5,O6) used to form the single OR gate (In17, In18) to get output(O7). The logic timing diagram is used to form the flow chart and 3-pin XOR gate. The schematic 3 input XOR gate has low delay and high switching speed. Also the threshold power is low in this 3 input XOR logic Gate. The (3 input XOR) logic gate has truth table is shown. The Table1shows the 3 pin xor gate input and the output by using the switch in the circuit.

Table 1 3 input Xor gate Truth table

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In1	In2	In3	output
0	0	0	0
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

(In1,In2,In3),(In4,In5,In6),(In7,In8,In9),(In10,In11,In12) are connected with (S1,-S1),(S0,-S0),(S1,-S0),(-S0,-S1) are connected with NOT gate to form the multiplexer also with 2 input XOR gate is shown in fig 1.

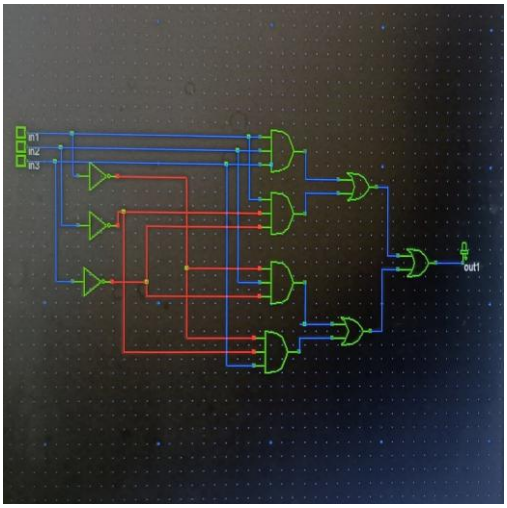

Fig:1 3 input xor gate

The logic gates are used for less propagation delay and threshold voltage. The power consumption of the 3input Xor gate is less. So , the Xor gate is used in timing and regulator purposes. By designing the 3 input xor gate is used to reduce the power consumption during output region. The switching speed is increases by using multiple pin logic gate, because the two pin has lesser comments is input to the logic gate but we give 3 input logic gate,it will used to give multiple comments to the output system.

By increasing the pins in the logic gate, it will leads to increase complex pipelining is formed and multiple tasks are formed in a single chip.

Output for the 3 pin xor gate

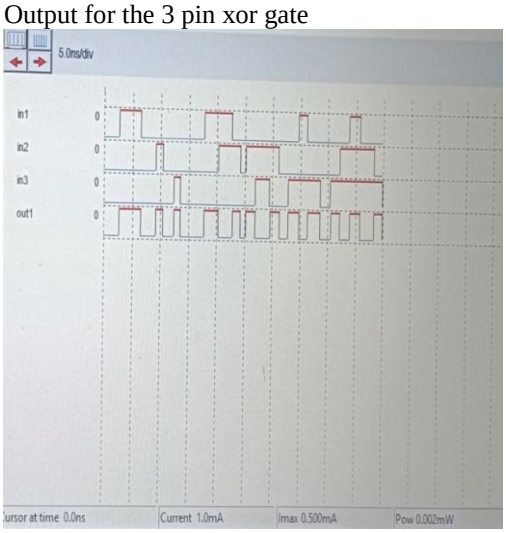

Fig:2 output for 3 input Xor gate

The output timing diagram for 3 input Xor gate is shown in fig 2 also the switching of three input and output time and power is shown.

XOR/XOR MULTIPLIER

To form the 4:1 multiplier is designed by using XOR gate. The XOR/XOR Multiplier is formed by using the switch supply and the timing diagram is s hown in fig 3,

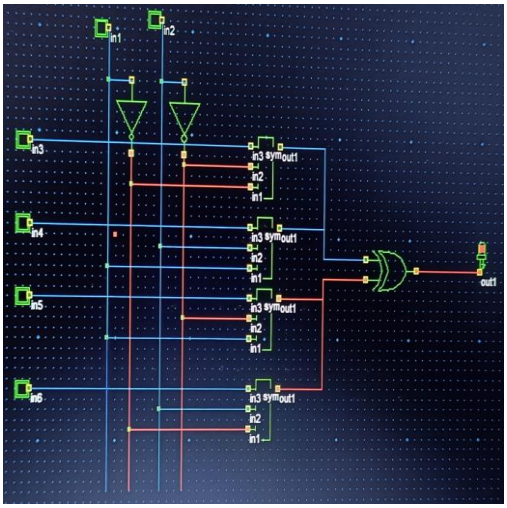

Fig:3 4 Pin XOR/XOR MULTIPLIER

XOR/XNOR MULTIPLIER

To form the 4:1 XOR/XNOR multiplier is designed by using by using (3 input XOR) and (2 input XNOR gate)is designed ,also the timing diagram is plotted .

The difference between the multiplier of XOR/XOR and XOR/XNOR is designed. The truth table is plotted by using

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schematic diagram of XOR/XOR and XOR/XNOR is designed. Also the truth table is shown in table 2.

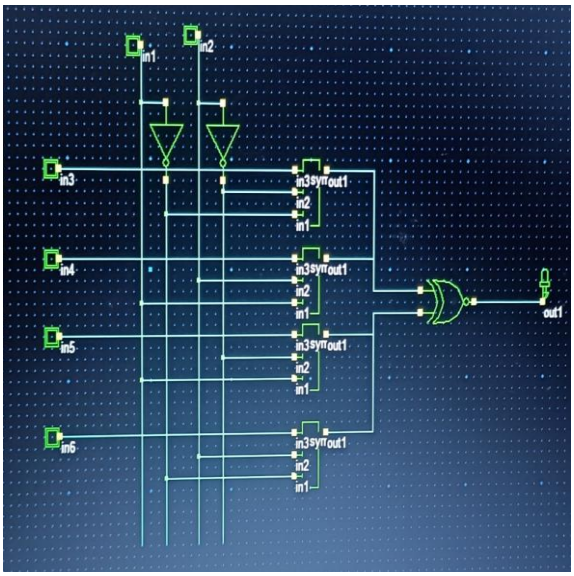

Fig:4 4 Pin XOR/XOR MULTIPLIER

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The 3 input xor/xnor multiplier is connected with 2 input inverter NOT gate and output is plotted also the diagram of 3 input xor/xnor mux is shown in fig 4,
Also the xor\xor mux gate has been designed with 4 pin input and 2 inverter pin in the circuit. The schematic diagram is shown in fig 5,

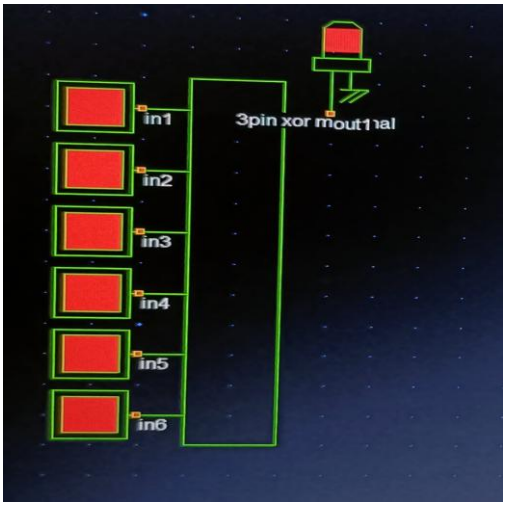

Fig:5 Schematic Diagram of Xor logic gate

Also the xor\xnor mux gate has been designed with 4 pin input and 2inverter pin in the circuit. The schematic diagram shown in fig 6,

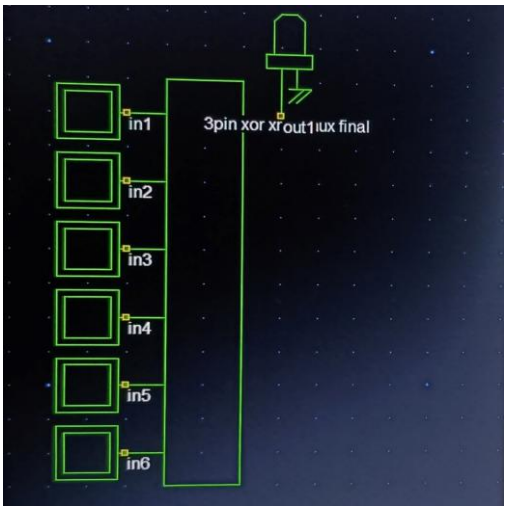

Fig:6 Schematic Diagram of Xnor logic gate

com	In1	In2	In3	In4	In5	In6	Output (3 pin xor/xor gate)	output (3 pin xor xnor gate)
1	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	1
3	0	1	0	0	0	0	1	0
4	0	0	1	0	0	0	1	0
5	0	0	0	1	0	0	0	1
6	0	0	0	0	1	0	1	0
7	0	0	0	0	0	1	1	0
8	1	1	0	0	0	0	0	1
9	1	0	1	0	0	0	0	1
10	1	0	0	1	0	0	1	0
11	1	0	0	0	1	0	0	1
12	1	0	0	0	0	1	0	1
13	0	1	1	0	0	0	1	0
14	0	1	0	1	0	0	0	1
15	0	1	0	0	1	0	1	0
16	0	1	0	0	0	1	1	0
17	0	0	1	1	0	0	0	1
18	0	0	1	0	1	0	1	0
19	0	0	1	0	0	1	1	0
20	0	0	0	1	1	0	0	1
21	0	0	0	1	0	1	0	1
22	0	0	0	0	1	1	1	0
23	1	1	1	0	0	0	0	1
24	1	0	1	1	0	0	1	0
25	1	0	0	1	1	0	1	0
26	1	0	0	0	1	1	0	1
27	0	1	1	1	0	0	0	1
28	0	1	0	1	1	0	0	1
29	0	1	0	0	1	1	1	0
30	0	0	1	1	1	0	0	1
31	0	0	1	0	1	1	1	0
32	0	0	0	1	1	1	0	1
33	1	1	1	1	0	0	1	0
34	1	0	1	1	1	0	1	0
35	1	0	0	1	1	1	1	0
36	0	1	1	1	1	0	0	1
37	0	1	0	1	1	1	0	1
38	0	0	1	1	1	1	0	1
39	1	1	1	1	1	0	1	0
40	1	0	1	1	1	1	1	0
41	1	1	0	1	1	1	1	0
42	1	1	1	0	1	1	0	1
43	1	1	1	1	0	1	1	0
44	1	1	1	1	1	1	1	0

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Table:2 Truth Table for xor/xor ,xor/xnor logic gate

SOFTWARE

DSCH Microwind is principally digital schematic circuit designing software. This is microwind simulation software which allows the addicts to pretend and design intertwined circuit at physical description position. This is stoner friendly circuit simulation software and it supported by huge symbol libraries. Microwind unifies schematic entry, pattern rested simulator, SPICE birth of schematic, Verilog extractor, layout compendium, on layout mixed- signal circuit simulation. Microwind software helps to design colorful types of sense gates AND, OR, NOR, NAND, XOR and numerous advanced design included with half adder, full adderetc. The DSCH program is a sense editor and simulator. Microwind EDA software is used to design and stimulate the 3 input Xor gate using AND, OR and NOT gate. Where the complex circuit is used to design the complex Xor and Xnor mux. And the verity table and the Timing illustration for the for the mux is designed.

Output for xor/xor mux

The output timing diagram and threshold power xor/xor is shown in fig 7. The three input and single output is plotted by switching the circuit in the output diagram.

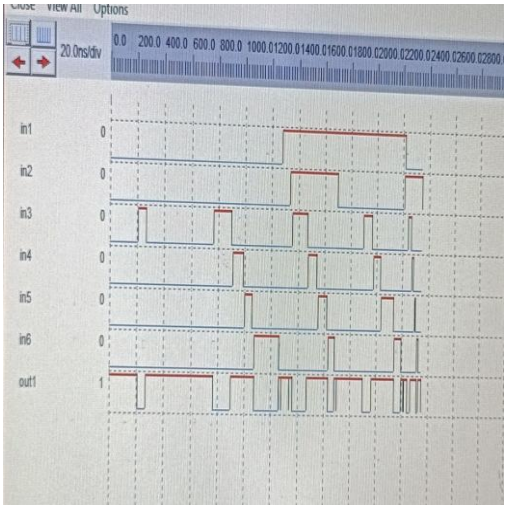

Fig:7 Output for xor mux

Output forvxor/xnor mux

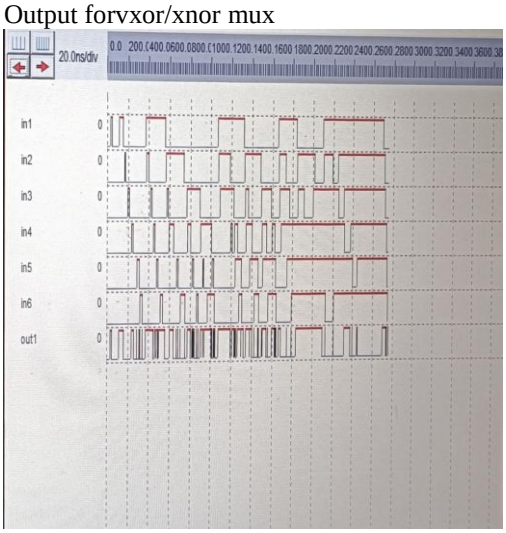

Fig:8 Output for xnor mux

The output timing diagram and threshold power xor/xnor is shown in fig 8. The three input and single output is plotted by switching the circuit in the output diagram.

STIMULATION AND RESULT:

Where the current, maximum current in grid power loss, power consumption and ns per division is compared in the table3,

TABLE 3:

VALUES	CURRENT	IMAX	POWER	NS/DIV
3PIN CMOS	4mA	12mA	1.5 mv	10ns
3PINXOR GATE	1mA	0.5mA	0.002mv	5ns
3PINXOR/XOR MUX	5mA	1.202 mA	0.002mv	20ns
3PIN XOR/XNOR MUX	5mA	2mA	0.11 mv	20ns
3 PIN CMOS MUX	10mA	29.6mA	0.7 mv	25ns

The a) as the output diagram of 3 pin xor/xor mux,
b) as the output diagram of 3 pin xor/xnor mux,
c) as the ouput diagram of 3 pin xor logic gate,
d) as the output diagram of 3 pin cmos,
e) as the output diagram of 3 pin cmos mux,

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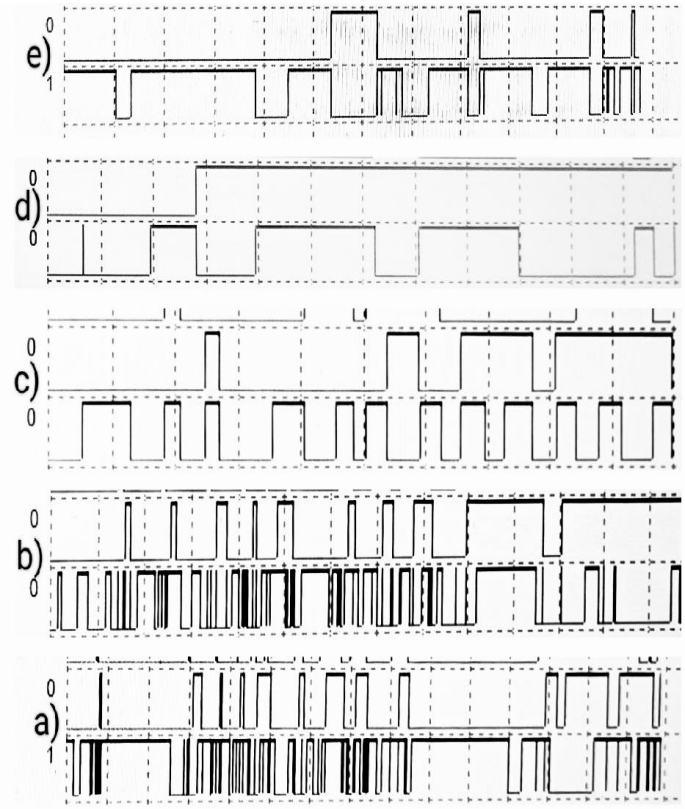

Fig:9 output power and delay diagram

CONCLUSION

The 3T based 4:1 Xor/Xor multiplier and 4:1 xor/Xnor multiplier is designed for low power consumption in transmit of signal compared to cmos multiplier. so, the xor/xor and xor/xnor mux is designed to compare the power loss and propagation delay. The truth table and timing diagram is plotted in this paper. The Microwind 3.9 EDA Software is used for this paper.

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