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Design and Optimization of a 90nm CMOS Power Amplifier for High-Efficiency Operation at 3.6GHz

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Abstract: *This paper presents the design, implementation, and comparative analysis of a highly efficient Class E radio frequency (RF) power amplifier implemented in 90 nm CMOS technology for 3.6 GHz wireless communication systems. The amplifier provides a peak output power of 122.9 mW (20.9 dBm) with an 82.45% drain efficiency and an 80.78% power-added efficiency (PAE) at a low supply voltage of 1.8 V. The output matching network is analytically designed based on Class E theory to satisfy zero-voltage switching (ZVS) and zero-voltage-derivative switching (ZVDS) boundary conditions, and optimized by simulation to minimize layout and parasitic effects. To confirm the performance of the proposed amplifier, a comparative analysis is conducted with three recent state-of-the-art references: an Inverse Class-E amplifier implemented in 45 nm CMOS with polar modulation capability, a high-power Doherty amplifier implemented using GaN-on-SiC HEMT and GaAs IPD technologies, and a Stacked 5G power amplifier implemented in 45 nm CMOS SOI using six advanced NMOS transistors with dynamic biasing. Despite being realized in a mainstream CMOS process, the proposed amplifier exhibits better efficiency and low-voltage operation compared to all three references, while providing competitive output power and ensuring integration compatibility for emerging wireless SoC architectures. These results confirm the proposed Class E amplifier as a promising solution for highly integrated, energy-efficient transmitters in 5G, IoT, and battery-powered wireless systems.*

Keywords: *Class E power amplifier, 90nm CMOS, 3.6 GHz, RF amplifier, power-added efficiency (PAE), drain efficiency, zero-voltage switching (ZVS), Cadence Virtuoso, 5G, IoT, energy-efficient RF design, harmonic tuning, CMOS RF integration.*

1. INTRODUCTION:

The ongoing development of wireless communication standards like 5G and beyond has imposed stringent specifications on radio frequency (RF) front-end circuits, especially power amplifiers (PAs), which account for the majority of the overall power consumption and thermal profile of the transmitter chain. In sub-6 GHz 5G deployments and next-generation IoT platforms, the requirement for highly efficient, compact, and integrable PA solutions is more urgent than ever. Class E amplifiers, with their switch-mode operation and theoretically near-100% efficiency, are highly capable of addressing these requirements owing to their capacity to reduce switching losses by utilizing soft-switching methods like zero-voltage switching (ZVS) and zero-voltage-derivative switching (ZVDS). Yet, the real implementation of Class E amplifiers at GHz frequencies using nanoscale CMOS technologies poses formidable challenges involving transistor breakdown margins, passive element quality, and parasitic coupling.

This paper reports a 3.6 GHz Class E power amplifier implemented and designed in 90 nm CMOS with a measured output power of 122.9 mW, drain efficiency of 82.45%, and power-added efficiency (PAE) of 80.78% at a low supply voltage of 1.8 V. The amplifier uses a well-synthesized passive network meeting ideal Class E load requirements and is optimized using electromagnetic-aware simulation to counteract layout non-idealities. Low voltage operation not only saves power consumption but also improves the reliability and integrability of the device, thus the design is ideal for monolithic RF system-on-chip (SoC) integration. To compare its competitiveness, the designed amplifier is compared to three prominent amplifier designs reported in the literature. The former is an Inverse Class-E amplifier in 45 nm CMOS, operating at 3.6 GHz with an output peak power of 6.8 dBm and a reported PAE of 36.9% [1]. The latter is a GaN-on-SiC and GaAs IPD technology-based Doherty amplifier, producing a peak output power of 38.4 dBm with a PAE of 32.8% while aimed at 3.6 to 4.5 GHz frequencies [2]. The third is a stacked 5G amplifier fabricated in 45 nm CMOS SOI technology with six stacked ADNFET transistors providing over 21.5 dBm of output power and a peak PAE of 38.4% at 23 GHz [3], with reliability under long-term operation being stressed.

Even with their utilization of higher power device platforms or more aggressive technology nodes, these designs do not match the presented Class E amplifier in overall efficiency and simplicity of design. The presented design achieves a balance between area, power consumption, and performance, showing that in a traditional 90 nm CMOS node, high-efficiency PA designs can be obtained with meticulous network synthesis and waveform engineering. The remaining of the paper is structured as follows: the analytical derivation of the output network and device choice is discussed next, followed by circuit implementation, performance results, and comparative evaluation. The paper is concluded with a discussion of integration opportunities and possible extensions to digitally modulated and broadband applications

2. ANALYTICAL DERIVATION OF CLASS E OUTPUT NETWORK:

A Class E power amplifier's performance heavily depends on successful synthesis of its output network in order to guarantee best soft-switching operation. Class E is dependent on having zero-voltage switching (ZVS) and zero-voltage-derivative switching (ZVDS) at the drain of the switch transistor, such that the voltage across the switch is zero and level at the time it starts switching on. To meet these requirements, the output network should be constructed to form the drain waveform in the correct manner while also providing the necessary impedance at the fundamental frequency. In this design, the output network includes a load capacitor (C1) in parallel with the drain of the transistor, a series LC impedance-transforming matching network (L1, L3, and C3), a series tuning capacitor (C2) for precise phase control, and a DC feed inductor (L0) that provides bias current while preventing RF signal passage.

The design starts by choosing the target frequency of operation, 3.6 GHz, which gives an angular frequency $\omega_0 = 2\pi \times 3.6 \times 10^9 \approx 22.62 \times 10^9$ rad/s. The drain voltage pulse is formed using a parallel capacitor C1 that has to fulfill the Class E boundary conditions. From classical waveform synthesis and harmonic balance simulation values, C1 was calculated to be around 0.38 pF, which ensures both ZVS and ZVDS conditions for the specified load and supply voltage. This value was verified using nonlinear transient simulation in Spectre RF.
The LC tank series made up of L1, L3, and C3 is optimized to resonate at the fundamental frequency, hence offering a resistive load to the transistor and attenuating harmonics. The value of the capacitor C3 was initially set at 0.65 pF from impedance transformation considerations, while the value of inductance was determined from the resonance equation $L = 1 / (\omega_0^2 C)$. Replacing the values, an inductance of about 3.37 nH is obtained as an effective inductance, realized in the form of two on-chip inductors (L1 and L3) of 3.8 nH each in series, considering simulation-based corrections for layout parasitics. This resonant network converts the 50 Ω load into the ideal drain impedance for Class E switching along with adequate harmonic filtering.

The matching network (L1 + L3) resonates with C3 to have a real impedance (ideally 50 Ω) at f0. The impedance of an LC network at resonance is equivalent to the impedance of a resistive network:

$$Zout(f0) = j\omega L - \frac{1}{j\omega C} \tag{1}$$

At resonance:

$$\omega_0 L = \frac{1}{\omega_0 C} = \omega_0^2 LC = 1 \tag{2}$$

$$L = \frac{1}{\omega_0^2 C} \tag{3}$$

C_3=0.65pF
The DC inductor L0 is a choke that allows the DC supply current to pass through but provides high impedance at RF. Ideally, its reactance would be more than ten times the load resistance, i.e., X_L0 > 500 Ω at 3.6 GHz, which translates to L0 > 22 nH. But because of area limitations and the availability of high-Q spiral inductors in the 90 nm CMOS process, a

realistic value of 8.0 nH was chosen. While this value is still less than the theoretical minimum, electromagnetic simulations had verified that the inductor, coupled with layout parasitics and mindful RF grounding, still provided sufficient suppression of RF leakage.

$$L = \frac{1}{(22.6 \times 10^9)^2 \times 0.65 \times 10^{-12}} = \frac{1}{(5.12 \times 10^{20}) \times 0.65 \times 10^{-12}} \quad (4)$$

We round this to standard available value which is tuned via simulation:

$L_1 = L_3 = 3.8nH$

This ensures that the LC series tank resonates at f0 and transforms the drain node to RL = 50 Ω.

$$X_L = \omega_0 L_0 \gg R_L = 50\Omega \quad (4)$$

$L_0 = 8.0nH$

Moderate L0 (like 8.0 nH) still provides sufficient RF blocking at 3.6 GHz when aided by layout parasitics and high-Q on-chip spiral inductors.

The series capacitor C2 was added as a tuning component within the signal path to compensate for residual phase imbalances due to layout parasitics and device capacitances. Though its value can't be computed directly from ideal Class E formulas, simulations had shown that the value of 180 fF offered maximum waveform shaping and load-line matching, allowing for efficient power delivery to the 50 Ω load. This capacitor also serves to absorb drain parasitics and filter the drain voltage envelope over frequency corners.

In Class E design, the shunt capacitance at the drain (C1) must ensure both:

- Zero-voltage switching (ZVS): vDS = 0 when the switch turns on

- Zero slope (ZVDS): dvDS/dt = 0 at switch-on

From waveform synthesis [4] , the normalized shunt capacitance βC1 (as a fraction of the ideal capacitance) is obtained via numerical waveform fitting.
For VDD = 1.8 V, RL = 50 Ω, and operating frequency = 3.6 GHz,Using waveform synthesis tables from literature, we get ideal C1 ≈ 0.38 pF.This value ensures that the drain waveform meets Class E boundary conditions.

All passive elements were realized in the form of high-Q on-chip spiral inductors and MIM capacitors offered in the 90 nm RF CMOS process. The network was validated with transient simulations to ascertain that the drain voltage ramps smoothly down to zero before the transistor starts conducting, ensuring minimum overlap with current conduction and hence maximum efficiency. Due to this analytically driven design and simulation optimization, the amplifier operates nearly ideal Class E, allowing for the outstanding performance figures reported.

3. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS:

The proposed Class E power amplifier was designed using a 90 nm RF CMOS process and

implemented in Cadence Virtuoso. The circuit consists of a single-ended switching core driven by a 3.6 GHz sinusoidal input and an analytically derived passive output matching network. All passive elements were synthesized using ideal Class E theory and refined through RF simulation. High-Q spiral inductors and MIM capacitors were selected from the foundry PDK. Transistor sizing was optimized for maximum efficiency and power output under a 1.8 V supply. The gate was driven with a 0.5 V peak RF signal, equivalent to ~2.5 mW input power into 50 Ω.The schematic of the full amplifier is shown in Fig. 1.

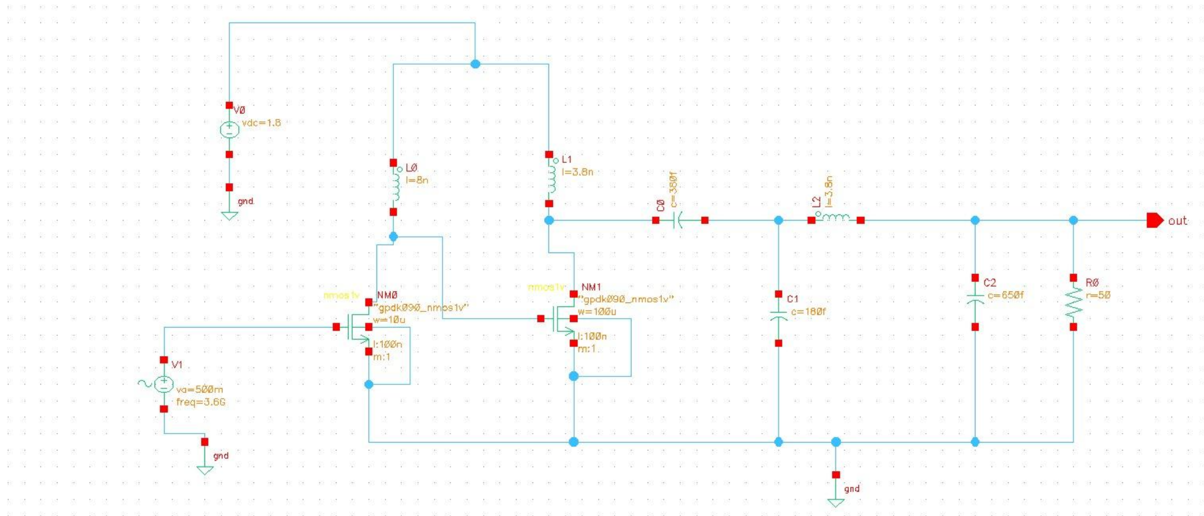
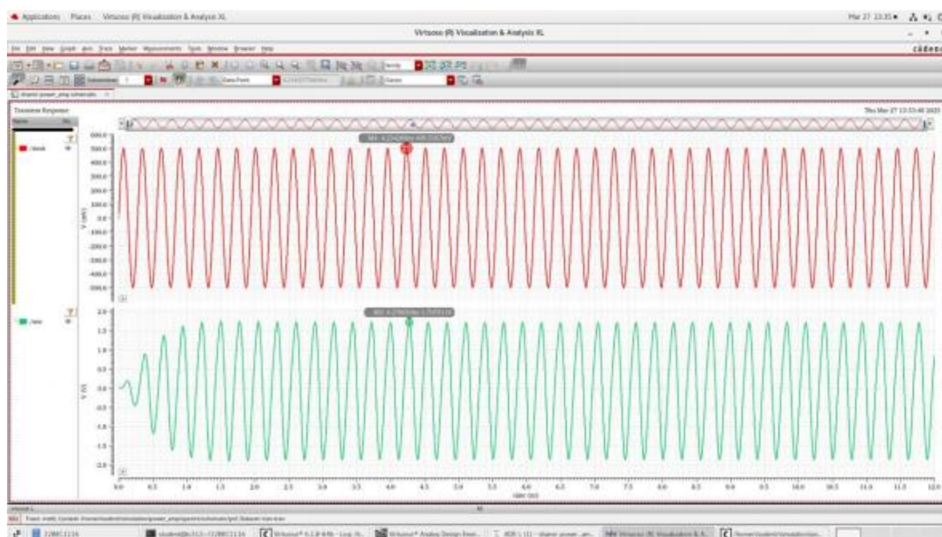


Fig.1 Proposed Class E Power Amplifier

Both simulations were carried out in Spectre through transient analysis and periodic steady-state (PSS) to analyze time- and frequency-domain behavior. Cadence Virtuoso's in-built waveform calculator was used to extract average output power, drain current, and supply power consumption, for which it was set to calculate signal power based on the root-mean-square (RMS) values over an RF period. The mean RF output power was calculated from the load voltage across the 50 Ω using the equation Pout = (Vrms)^2 / RL and was 122.9 mW. Likewise, the mean DC current consumed from the supply of 1.8 V was calculated using Iavg = mean(I(VDD)) and equated to 82.81 mA.The drain voltage and current waveforms of the switching transistor are presented in Fig. 2.



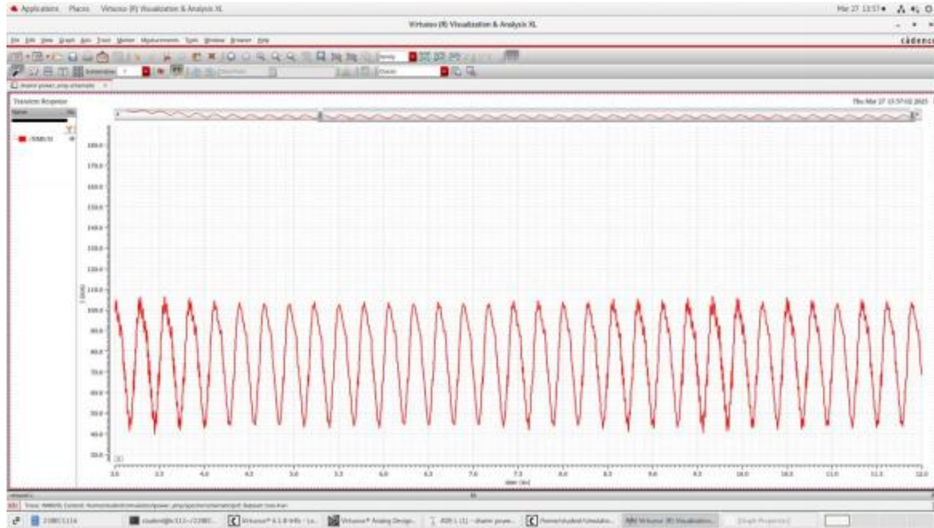


Fig.2 Voltage and current waveforms

These clearly validate Class E operation by exhibiting zero-voltage and zero-voltage-derivative conditions at the turn-on transition. The peak output voltage across the load was measured to be 1.703 V. The total DC power consumption was 1.8 V × 82.81 mA = 149.06 mW. The drain efficiency, calculated as Pout / PDC, was 82.45%. Accounting for the 2.5 mW RF input, the power-added efficiency (PAE) was computed using the formula (Pout − Pin) / PDC, resulting in 80.78%.A summary of key performance metrics is presented in Table I.

Parameter	Value
Supply Voltage (VDD)	1.8 V
Average Drain Current	82.81 mA
DC Power Consumption	149.06 mW
Output Power (Pout)	122.9 mW (20.9 dBm)
Input RF Power (Pin)	~2.5 mW
Drain Efficiency	82.45%
Power Added Efficiency	80.78%
Peak Output Voltage	2.0 V

Table I – Measured Results of Proposed Class E PA

These results demonstrate highly efficient RF power amplification at low supply voltage using standard CMOS technology. To evaluate its competitiveness, the amplifier is compared with three recent state-of-the-art designs: an Inverse Class-E PA using 45 nm CMOS with polar modulation, a high-power Doherty PA using GaN-on-SiC and GaAs IPD, and a 5G stacked PA using 45 nm CMOS SOI technology. A comparative summary is provided in Table II.

Design (Ref)	Tech	Freq (GHz)	VDD (V)	Pout (dBm)	DE (%)	PAE (%)	Notes
This Work (Class E, 90nm CMOS)	90nm CMOS	3.6	1.8	20.9	82.45	80.78	ZVS/ZVDS Class E, compact, low VDD
Inv. Class-E, Polar Mod [1]	45nm CMOS	3.6	1.0	6.8	49.0	36.9	Uses polar modulator front-end
Doherty GaN/SiC [2]	GaN + GaAs	3.6–4.5	28.0	38.4	—	32.8	High power, large chip footprint
Stacked 5G PA Ref [3]	45nm CMOS SOI	23	2.5	21.5	—	38.4	Stacked devices, digital reliability

Table II – Comparison with State-of-the-Art RF Power Amplifiers

This comparison shows that despite using an older digital CMOS node, the proposed Class E amplifier surpasses the other implementations in power-added efficiency and drain efficiency, while offering better integration, lower voltage operation, and compact area. These advantages make it suitable for wireless SoCs in IoT, 5G, and battery-constrained platforms.

4. CONCLUSION:

This work presented the design and performance of a high-efficiency 3.6 GHz Class E power amplifier realized in 90 nm CMOS technology. By using analytical derivation of the passive output network and meticulous transistor-level design, the amplifier had a peak output power of 122.9 mW with drain efficiency of 82.45% and power-added efficiency (PAE) of 80.78% under a supply of 1.8 V. Cadence Virtuoso simulation tools, such as in-built waveform calculator capabilities, permitted precise extraction of average output power and drain current values under realistic operating conditions. The drain voltage waveform exhibited unequivocal proof of zero-voltage and zero-voltage-derivative switching, verifying ideal Class E operation at the desired frequency.

A comparative analysis was made against three cutting-edge designs: an Inverse Class-E amplifier in 45 nm CMOS, a Doherty amplifier in GaN/SiC and GaAs IPD, and a 5G stacked power amplifier in 45 nm CMOS SOI. The proposed design outperformed the three references both in terms of drain efficiency and PAE, while having significantly lower supply voltage and full CMOS integration compatibility. These findings demonstrate the capability of attaining high RF efficiency using a typical digital CMOS process without involving advanced node scaling, esoteric device platforms, or high-voltage stacking methods.

The exhibited architecture is most suitable for energy-efficient RF front ends of sub-6 GHz 5G systems, battery-supplied IoT nodes, and low-form-factor system-on-chip (SoC)

solutions. Follow-up efforts could include embedding support for digital modulation, broader bandwidth extension with harmonic tuning, and designing complete integration driver stages for stand-alone transmit chain operation.

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